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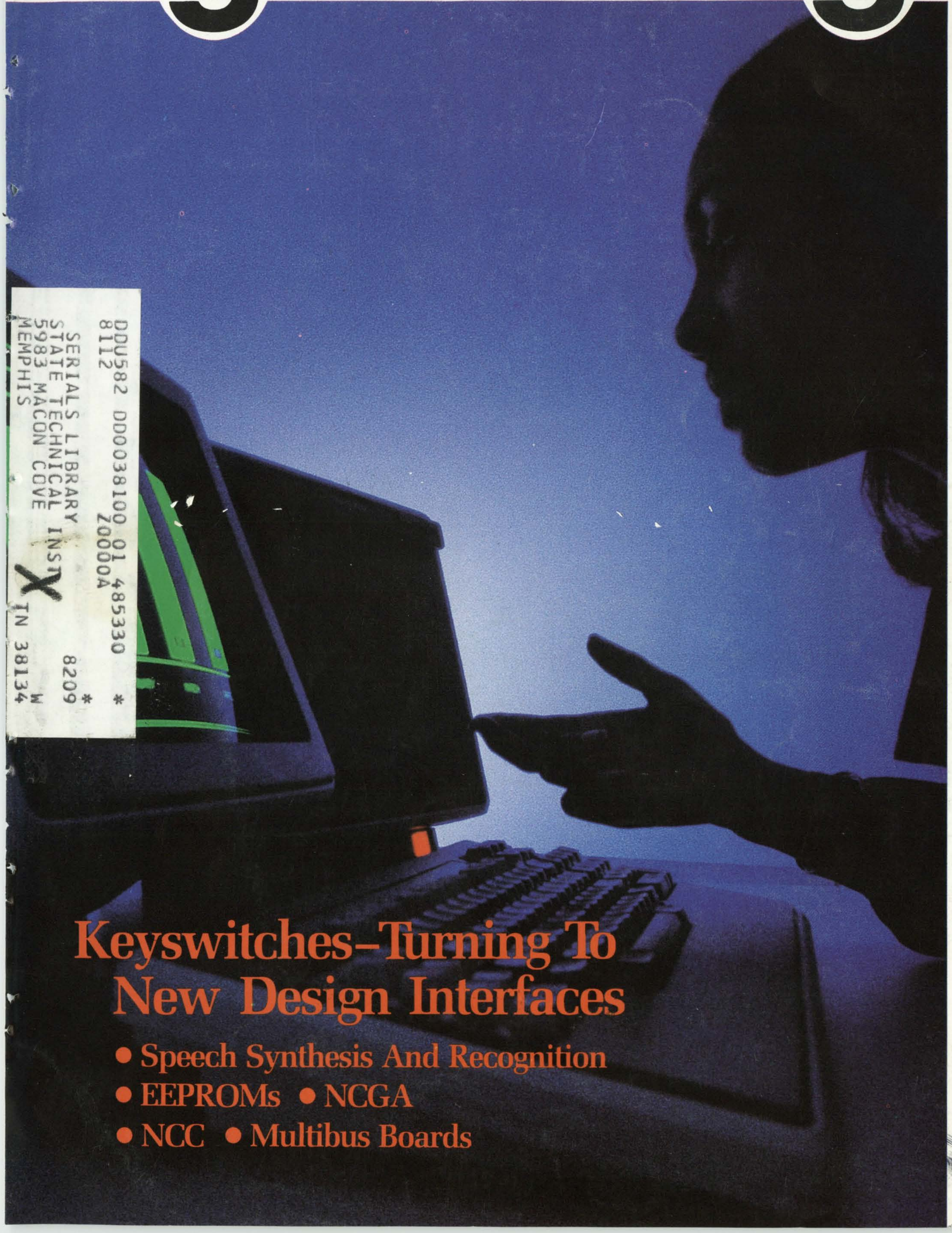

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Keyswitches–Turning To New Design Interfaces

- Speech Synthesis And Recognition
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- NCGA
- NCC
- Multibus Boards

COMPUTERS/SYSTEMS • PERIPHERALS • COMPONENTS • 5/82

VOL. 12
NO. 5

Only one company has the complete range of disks and disk backup—Kennedy

That's right. Ask any other supplier of peripheral products for system backup, and you'll find that some can supply a disk, some can supply a cartridge recorder, others a streaming transport. But none can supply the choice which Kennedy can offer.

Kennedy is the only company that can offer an SMD compatible, 8″ 40 MByte disk drive (Model 7300) and an 80 MByte 14″ Winchester disk drive (Model 5380). To back them up, Kennedy has a ¼″ cartridge recorder (Model 6450), and Model 6809, ½″ Data Streamer Tape Transport.

Kennedy was the first to utilize the ¼″ 3M cartridge for disk backup; Kennedy was the pioneer in Winchester disk technology, and was a leader in developing a low cost streaming tape drive.

All of these products were conceived and designed to meet the need for reliable, low cost backup — for our systems or for any other system.

Kennedy has always backed its products. That's why we're No. 1. Call or write us about your problem.

We won't back off.

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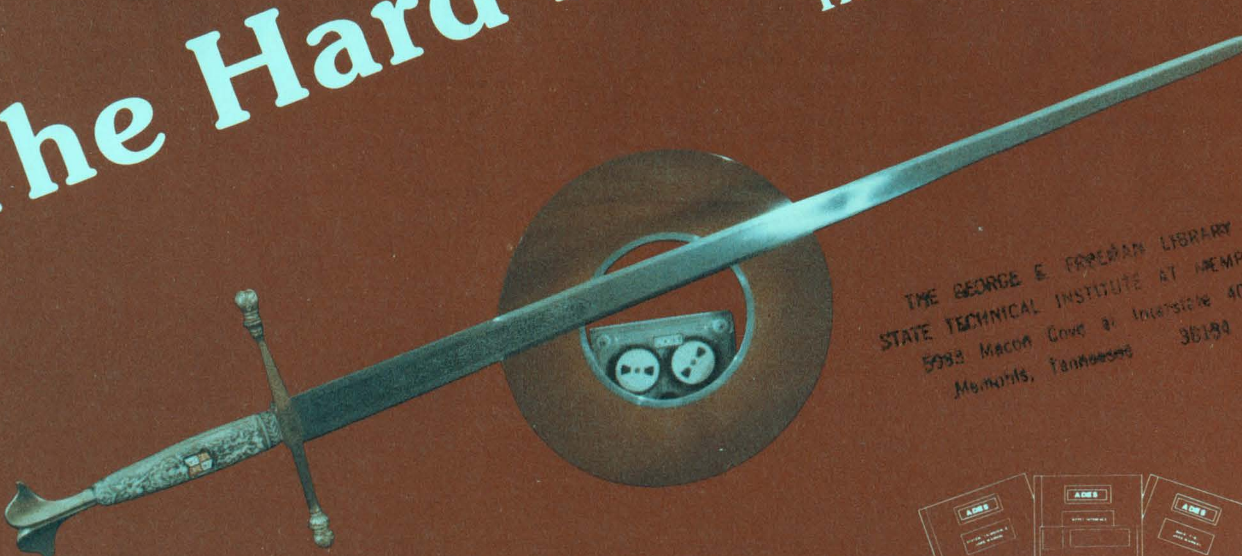
The Hard Edge in performance



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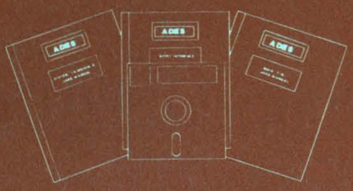

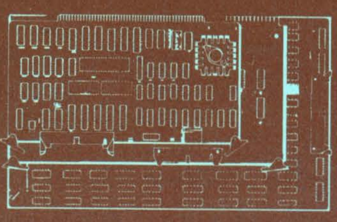

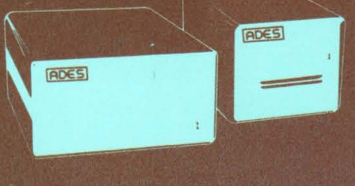

SYSTEMS

Whether you are a systems integrator or computer OEM, *ADES* subsystems provide the ultimate solution to your needs. As a fully supported product, *ADES* subsystems provide a revolutionary product capable of displacing cartridge disk drives and floppies.

SYSTEM 8

As a standalone table top or rackmount package, the *GYPSY* based SYSTEM 8 provides the user a disk of 10 MB, 34 MB, or 70 MB of disk capacity with 10 MB or 20 MB removability via the streaming tape.

SYSTEM 14

The *SYSTEM 14* provides 33 MB or 66 MB of disk storage with 20 MB removability via the streaming tape, disk tape packaging.

THE ULTIMATE SOLUTION

With all the performance of the *ADES GYPSY* controller, the *SYSTEM 8* or *SYSTEM 14* can meet your total memory subsystem requirements.

GYPSY

At the heart of the *ADES* product line is the *GYPSY* Winchester/Streaming Tape formatter. By combining the disk and tape functions into a single card, the *GYPSY* provides unprecedented system capabilities.

With a 5 Mbyte/minute offline disk to tape transfer rate, a user can backup or restore a 20 Mbyte logical drive in less than four minutes. When operating in the "Transparent Mode," the host can still access the disk while the *GYPSY* moves data between the disk and streaming tape. In multiuser systems, individual users can backup or restore logical elements without affecting other users on the system.

MORE THAN JUST BACKUP

Compiling the *GYPSY* disk/tape commands with the direct tape access commands provides a system capable of Operating System load, Program Exchange and Selective File storage and retrieval. The streaming tape thus provides more than just backup.

EASY INTEGRATION

The power and flexibility of the *GYPSY* is only surpassed by the ease of host integration. With as few as five 7400-type components, the *GYPSY* can be interfaced to most mini or microcomputers.

EXPANDING HARDWARE SUPPORT

ADES currently supports Priam and Century Data Disks in conjunction with DEI, Archive and Cipher ¼" cartridge streaming tapes.

SUPPORT

ADES supports the most widely used micro-computers, and their operating systems.

GYPSY HOST INTERFACE ADAPTERS (GHIAs)

For the user who desires to bring up his system quickly, *ADES* offers S100 and Multibus host adapters in both Programmed 1/0 and DMA configurations. In conjunction with *ADES* software, the *GHIAs* provide a rapid means of integration, with minimal effort.

THE Z80 CONNECTION

For the Z80-based systems, *ADES* provides the GHIA-Z80 which allows connection of *GYPSY, SYSTEM 8* or *SYSTEM 14* directly to the CPU, thus eliminating the problems of specialized base configurations.

SOFTWARE

ADES support of CP/M™ and MP/M™ makes the *GYPSY* and SYSTEMS 8 and 14 easy to integrate and use. Support levels range from the "non-programmer" and user to the systems integrator configuring high performance MP/M™ systems.

CP/M

The *ADES "BIOS ATTACH"* program allows a user to configure the program to his system configuration, and begin using the disk/tape subsystem as an integral system resource under CP/M 2.2.

MP/M

For the system integrator who must design a complete BIOS or XIOS, *ADES* supplies a series of detailed application notes. These publications allow quick and complete integration of *ADES* subsystems into all system applications.

UTILITIES

All disk/tape subsystems running with CP/M are also supported with an array of utility programs. Format and Verify, Defect Compensation and Backup and Restore are only a few examples.

See Us At
COMDEX
JUNE 28-30, 1982
Atlantic City Convention Hall
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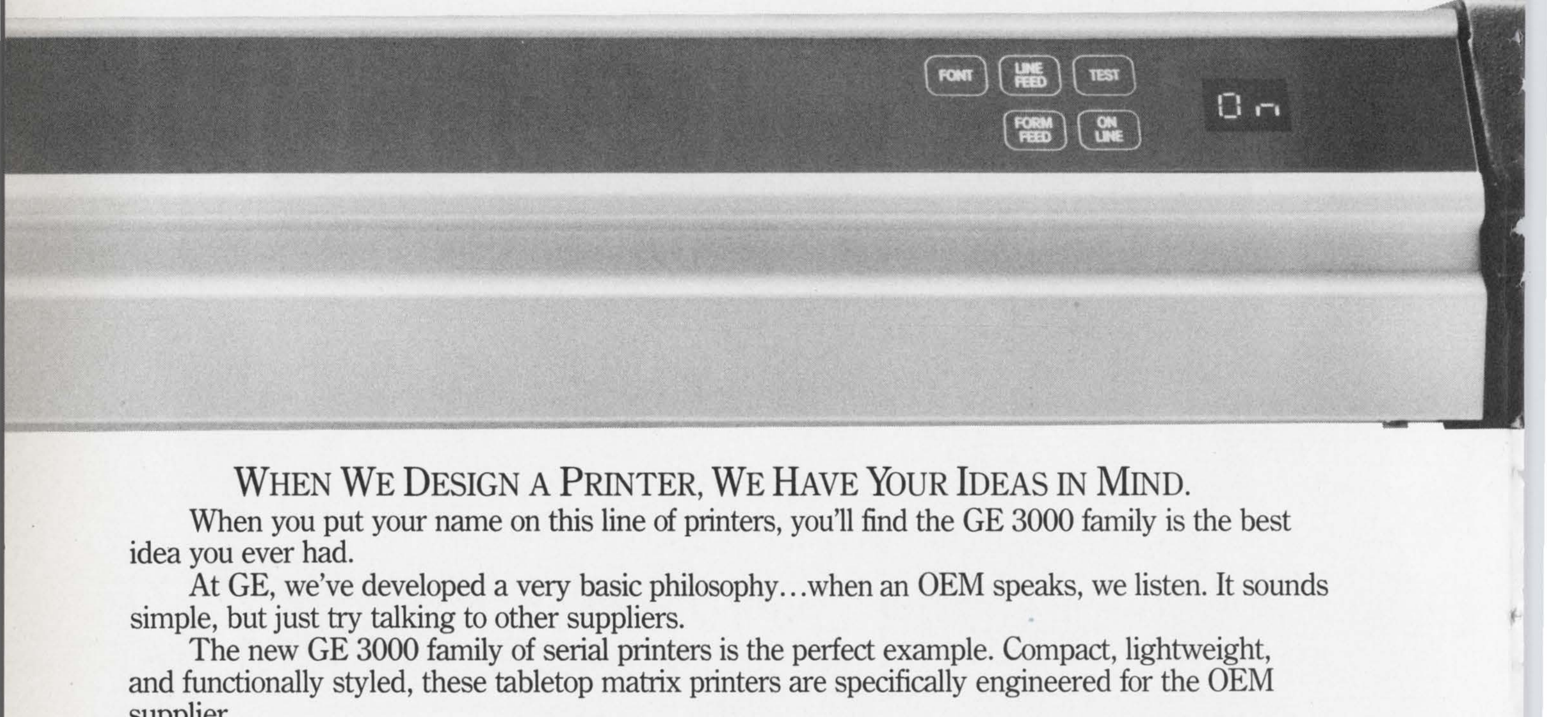
IT'S TIME YOU PUT YOUR NAME ON THE LINE.

Introducing the new GE 3000 family of printers.



WHEN WE DESIGN A PRINTER, WE HAVE YOUR IDEAS IN MIND.

When you put your name on this line of printers, you'll find the GE 3000 family is the best idea you ever had.

At GE, we've developed a very basic philosophy...when an OEM speaks, we listen. It sounds simple, but just try talking to other suppliers.

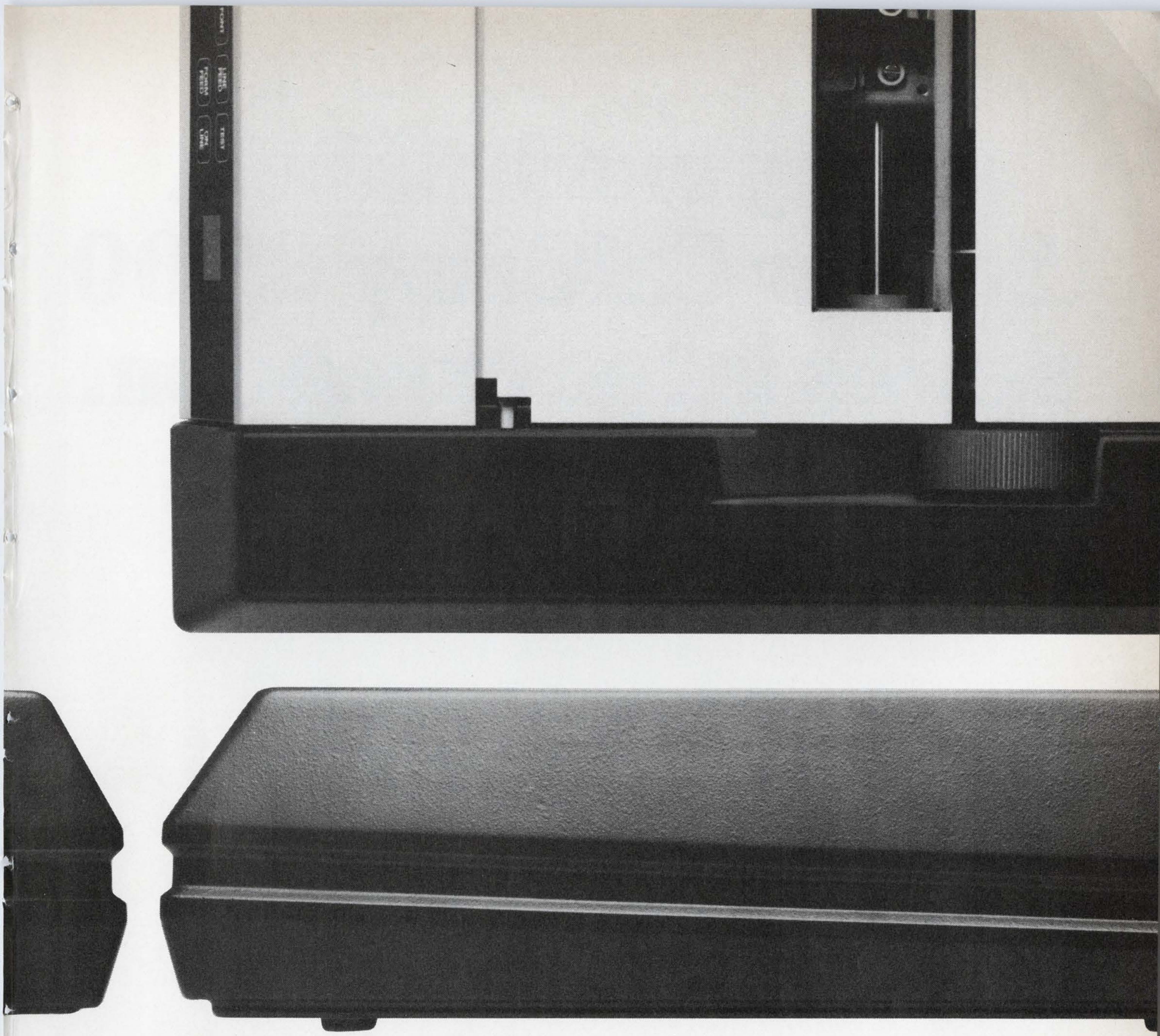
The new GE 3000 family of serial printers is the perfect example. Compact, lightweight, and functionally styled, these tabletop matrix printers are specifically engineered for the OEM supplier.

Our new line of six printer models offers cost effective solutions to virtually all your printing requirements. Standard print quality from 180 to more than 500 cps. Near letter quality from 100 to almost 200 cps. 80 and 136 column models.

A full range of standard features such as 72 × 72 dot/in. graphics with precision paper movement, self-threading paper load mechanism, close tear-off, six part forms capability, popular parallel and serial interface, and local and downline configuration selection with non-volatile storage. Plus a range of options and paper handling accessories for office and factory applications. And everything backed up by worldwide GE service.

NOW YOU CAN SOLVE YOUR CUSTOMER'S NEEDS EFFICIENTLY AND EFFECTIVELY.

The GE 3000 family is designed to offer OEM's the advantage of single-design simplicity...



without the application limitations of a single model product line.

The GE 3000 gives you configuration flexibility. Application flexibility. Design commonality and price/performance leadership.

OF COURSE, INNOVATIVE IDEAS ARE NOTHING NEW TO GE.

Our roots go back to Thomas Edison. It was in his tradition that in 1969 we introduced the first electronic data printer with modern LSI circuitry. Since then, we've continued in that inventive spirit, supplying OEM's with the finest in advanced printer solutions...longer than any other printer supplier.

General Electric. We're the industry leader in electronic printing. After all, we pioneered the industry in the first place.

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First In Electronic Printing.

See Us at NCC, Booth 1614

For the solution to your printing needs, call TOLL FREE 1-800-368-3182,
General Electric Company, Data Communication Products Department IN3S1, Waynesboro, VA 22980.
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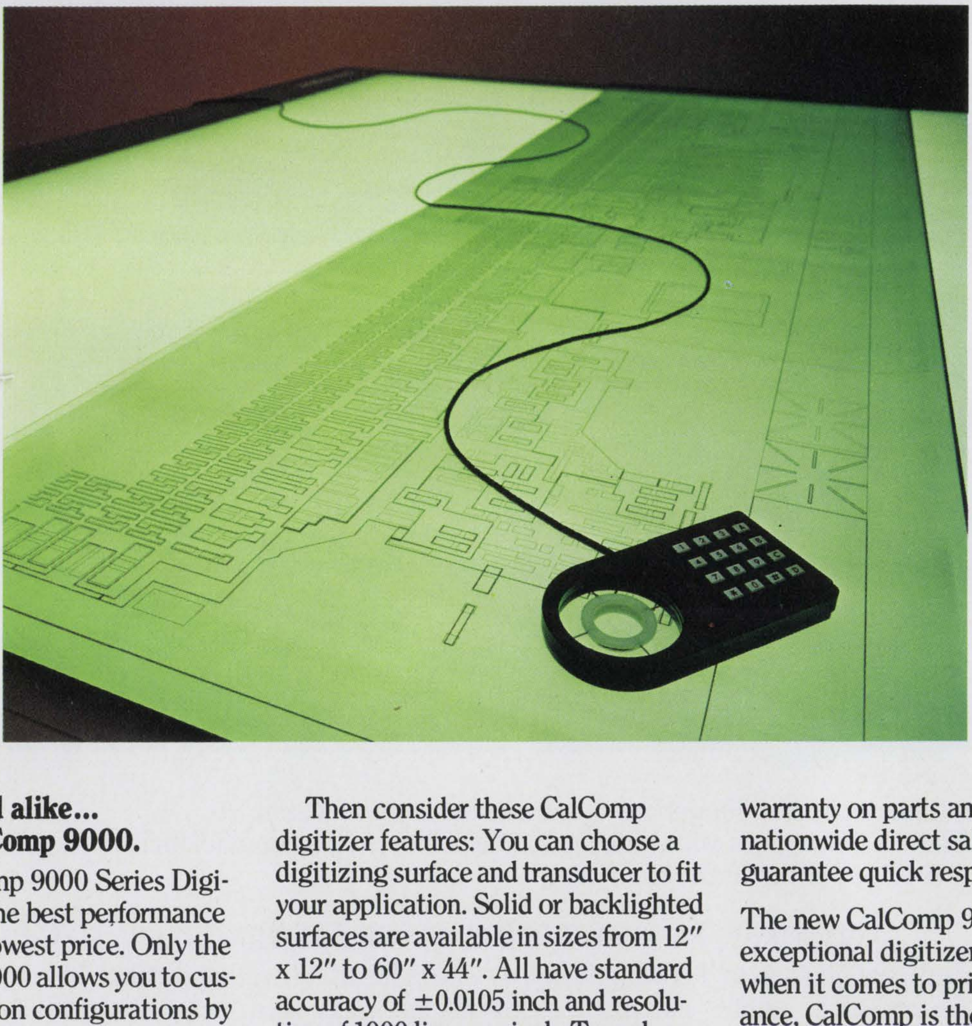
GENERAL ELECTRIC

Most digitizers are pretty much alike... the New CalComp 9000 Series is the exception.



Most are priced alike...
except the CalComp 9000.

The new CalComp 9000 Series Digitizer gives you the best performance features at the lowest price. Only the new CalComp 9000 allows you to customize application configurations by switch selectable character framing, data rate, operating modes and interfaces.

Most have the same features...
except the CalComp 9000.

Check the specs and you will find that accuracy, resolution, digitizing surface sizes and even transducers are just about the same on most competitive models.

Then consider these CalComp digitizer features: You can choose a digitizing surface and transducer to fit your application. Solid or backlighted surfaces are available in sizes from 12″ x 12″ to 60″ x 44″. All have standard accuracy of ±0.0105 inch and resolution of 1000 lines per inch. Transducer choices include a pen stylus, and 4, 12 or 16-button cursors.

The compatible 9000 Series lets you communicate simultaneously with several host computers and/or peripherals via multiple interfaces.

And, you can count on CalComp to keep your digitizer operating at peak efficiency. Each CalComp 9000 Series Digitizer carries a full one-year warranty on parts and labor. Reliable, nationwide direct sales and service guarantee quick response time.

The new CalComp 9000 Series is an exceptional digitizer. Point for point, when it comes to price and performance, CalComp is the choice.

Call or write today for complete specs on the 9000 Series.

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California Computer Products, Inc.
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Anaheim, California 92801
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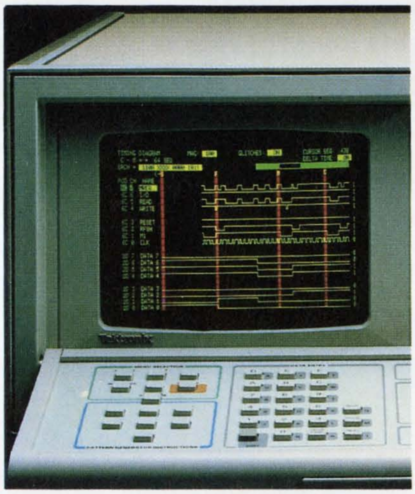

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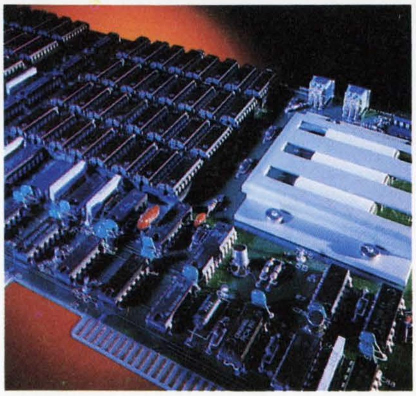

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WHY WAIT FOR THE FUTURE OF DISC STORAGE TECHNOLOGY TO REACH DEC SYSTEMS?

THE FUTURE IS AT PLESSEY. TODAY!

Plessey Peripheral Systems, the leader in low-cost, DEC-compatible data storage systems leads the way in Winchester technology.

NEW FROM PLESSEY

Plessey's new generation of 8-inch Winchester subsystems is the one complete solution for LSI-11 users. Configured as RK06 units, each drive provides you with 28 Mbytes of reliable, low-cost-per-bit storage. Each controller provides interface for up to four drives for a total system capacity of 112 Mbytes. Nearly triple the maximum subsystem capacity of an RL02*.

20% OFF STANDALONE Q-BUS WINCHESTER

8" Winchester for Q-bus 28 Mbytes or 56 Mbytes RK06

FSV06J

8-inch Winchester in self-contained chassis ends integration problems. 5-1/4" enclosure mounts easily in existing rack. Includes power supply. Quad-wide Q-bus controller. Emulates DEC RK611/RK06 disc subsystems.

FSV06J
$6,468
SAVE $1617

FSV06JJ
$10,812
SAVE $2703

FSV06JJ

Two 8-inch Winchesters in one ready-to-install chassis. Use one drive for backup. Or expand your existing LSI-11. Provides 56 Mbytes of storage. Fast transfer rate 912 Kbytes/second. An average seek time of 42msec. An outstanding buy at 20% off.

Plug one into your existing Q-bus backplane. Your new Winchester drive is housed in a slim 5 1/4-inch chassis for easy installation. . . . and you have your choice of Winchester/backup combinations.

Choose one or two Winchester drives. Winchester and floppy backup or Winchester and streaming tape backup.

You'll appreciate the reliability of Plessey's new Winchester subsystems. And save on maintenance costs, too.

Because the disc platters, read/write heads and positioners are sealed in a contamination-free environment, you eliminate the risk of head crashes.

Reduce periodic maintenance. No costly air filters to replace. No head alignments. No read/write adjustments.

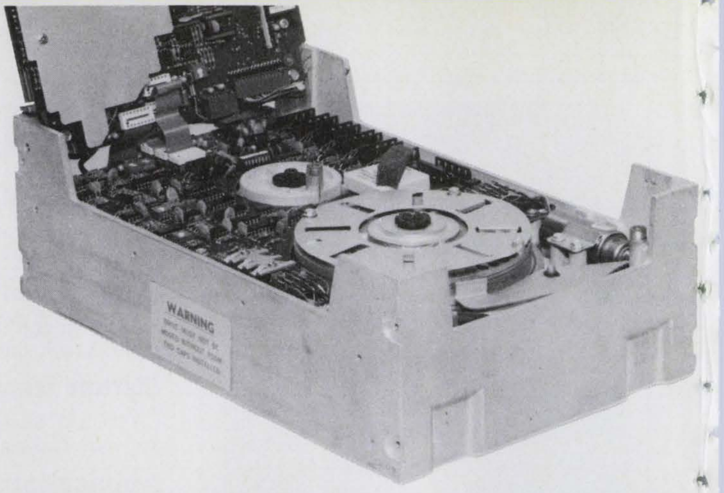
In addition, the clean recording environment allows closer tolerances in the positioning of the read/write heads. Yields greater recording densities. Higher transfer rates.

Compact
Reliable
Fast

No wonder the future belongs to Winchester disc drives.

No wonder Plessey is the recognized leader in DEC-compatible data storage systems.

OFFER



Q-BUS AND UNIBUS COMPATIBLE WINCHESTERS AND DEC-BASED COMPUTER SYSTEMS WITH WINCHESTER STORAGE AVAILABLE FROM PLESSEY PERIPHERAL SYSTEMS

NOW!

For years Winchester disc drives have been a common sight around large computer installations. Magnetic tape, used for archival storage, provided the backup required for the fixed media Winchesters.

FSV06ZJ
$7,964
SAVE $1991

FSV06ZJ

28 Mbyte fixed, Winchester storage and 1.2 Mbyte, double-sided, double density floppy for backup. Includes quad-wide Winchester controller. Dual-wide floppy disc controller. 5-1/4" chassis includes power supply

The same backup requirement stalled the use of Winchester technology in small minicomputer systems. Start-stop magnetic tape transports were too expensive for the small systems user. Floppy disc too slow.

Widespread use of 8-inch Winchester technology had to wait until someone solved the backup problem.

ANY WAY YOU ADD IT YOU'RE THE WINNER WITH WINCHESTERS FROM PLESSEY PERIPHERAL SYSTEMS

---

*Total RL02 capacity is 40 Mbytes

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ADD A WINCHESTER TO YOUR DEC SYSTEM ADD A WINNER FROM PLESSEY

INTRODUCING PLESSEY'S NEW 8″ WINCHESTER YOU SAVE 20% BY ORDERING NOW

EXTENDED

PLESSEY SOLVES THE BACKUP PROBLEM

Three years ago, Plessey Peripheral Systems set out to find the **ultimate** Winchester backup system.

The perfect solution would be simple to use. Fast. Inexpensive.

Two and a half years later, Plessey introduced its 1/4-inch streaming cartridge tape backup device — the PM-CSV11A.

It's simple to use
Fast
Inexpensive

So simple to use, in fact, a first-time user can perform backup routines within minutes. Effortlessly. Flawlessly.

ADD A WINCHESTER WITH FAST, EASY TO USE BACKUP

FSV06TJ
$8,496
SAVE $2124

FSV06TJ

Combines 28 Mbyte 8″ Winchester with 1/4″ streaming tape. Fast. Easy to use. True tape streamer — completes backup in 5 minutes. Operates at 90ips. NOT a TM11 or TU11 emulation. Unique. Convenient. Easy to handle tape cartridges cut media cost drastically. And store easily too.

Subsystem includes Winchester, tape streamer, power supply, chassis, controllers, and Cartridge Image Backup utility software.

Backup your new Winchester without interrupting your processor.

New on-line backup under RSX-11M allows file(s) transfer from fixed-media Winchester to ¼″ tape or complete disc backup to tape online (non-streaming). Only available from Plessey Peripheral Systems.

TRUE TAPE STREAMER

So fast you can backup an entire 28 Mbyte Winchester in 5 minutes.

Simply insert a tape cartridge. Type in a command and the tape drive does the rest. At 90 IPS you can backup an entire 28 Mbyte Winchester in 5 minutes. Each drive is partitioned into 14 Mbyte RK06 units for simple archival storage. Use your CSV11A to copy RK05s. RL02 packs. Supports TM11 mag tape.

Economical, too. Save on media costs. Load software and diagnostics. All for less than half the cost of a 1/2-inch tape transport.

20% SAVINGS ON PLESSEY'S UNIQUE SYST-23VTJ — THE MOST ADVANCED LSI-11/23 BASED SYSTEM ANYWHERE

23VTJ-320
$15,080
SAVE $3770

At 20% off, the most advanced LSI-11/23 based computer system just became the best priced. 28 Mbyte Winchester, 1/4-inch tape streamer, LSI-11/23 CPU with 128 Kbyte memory, serial line interface, 9-slot quad backplane in one desktop cabinet.

Enough computing power for eight users. Reliable Winchester storage. Easy to use streaming tape backup device that provides archival storage and software distribution.

That's advanced. But, there's more, Easily upgradeable with additional Winchester storage. And is fully supported by DEC or Plessey software. Nationwide Field Service. Ready for delivery. NOW.

OFFER ENDS JUNE 30

SAVE 20% DURING PLESSEY'S SPECIAL INTRODUCTORY OFFER

DD5/82

ADD A WINCHESTER, ADD A WINNER

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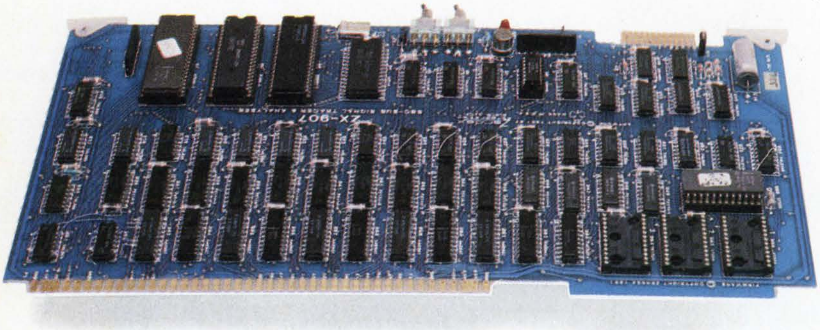
THE
ZENDEX ZX-907
BUS TRACER
Monitors Multibus* Operation

The ZX-907 represents a major advancement in Multibus development tools. This processor-based board, in conjunction with an external CRT, interprets Multibus events by monitoring address, data and control lines. The on-board memory will store up to 1024 bus events. The interpreted results are displayed on the CRT in the form of action, memory or I/O location, and data.

- **40 bit wide trace**
- **1024 Bus Cycle Storage in on-board RAM**
- **On-board 8085A-2 Processor**
- **Menu driven software trace control**
- **Breakpoint can be preset on Address =, <, >**
- **8 or 16 Bit Processor Compatibility**



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Tell us your thoughts

Digital Design is your forum — your inputs help keep the magazine interesting and vital to the design community. So let us know how we're doing and how we can serve you better in the future. We want to know what you like or dislike about *Digital Design*, the subjects you'd like to see us address, how you feel about the problems you face every day as design professionals.

If you have thoughts your peers should know about, put them in a letter in *Digital Design*. Have your say in *your* magazine! Send letters and comments to: Editor, *Digital Design*, 1050 Commonwealth Ave., Boston, MA 02215.

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PICK ANY TWO PERIPHERALS

5¼″ FLEXIBLE DISC DRIVE	8″ FLEXIBLE DISC DRIVE	¼″ CARTRIDGE TAPE DRIVE	5¼″ WINCHESTER DISC DRIVE	8″ WINCHESTER DISC DRIVE
SHUGART SA 400 SERIES OR EQUIV.	SHUGART SA 800R SERIES OR EQUIV.	KENNEDY D.E.I. QANTEX	C.M.I. R.M.S. SEAGATE SHUGART TANDON	CDC FINCH FUJITSU PRIAM QUANTUM SHUGART

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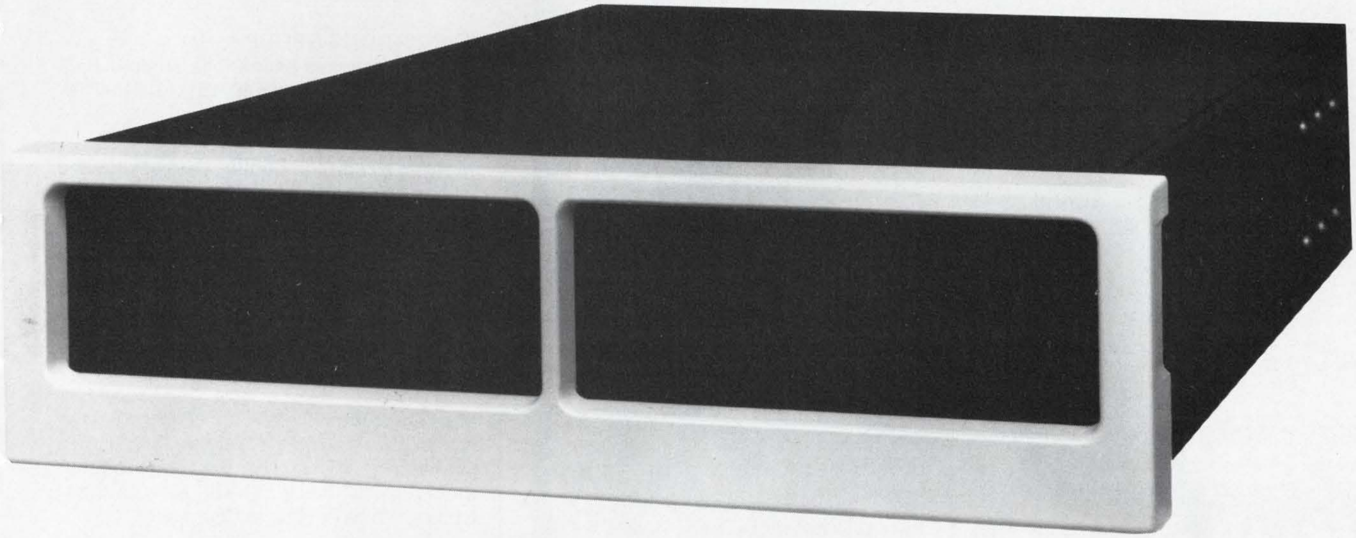

OPERATE!

Simple as that, you can have Winchester and/or back-up to 168 MB. That's because you've just met the Multi-Peripheral Chassis (M.P.C.)... the first dual peripheral housing *engineered* to simplify the difficult mixing or matching of data storage drives from several manufacturers.

Advantages you'll find in the M.P.C. include:

- Mounting holes are in the right place to accommodate the fractional size differences of the numerous drives.
- Power requirements of different drives are easily met by the flexible power system, which provides up to five voltages.
- Heat generated within the enclosure is reduced to safe drive temperature levels by the integral cooling system.
- Even troublesome safety and electrical interference problems have been minimized through use of proper grounding techniques.

But there's only one way to see how well the M.P.C. solves your data storage requirements with your CPU... simply contact DILOG.

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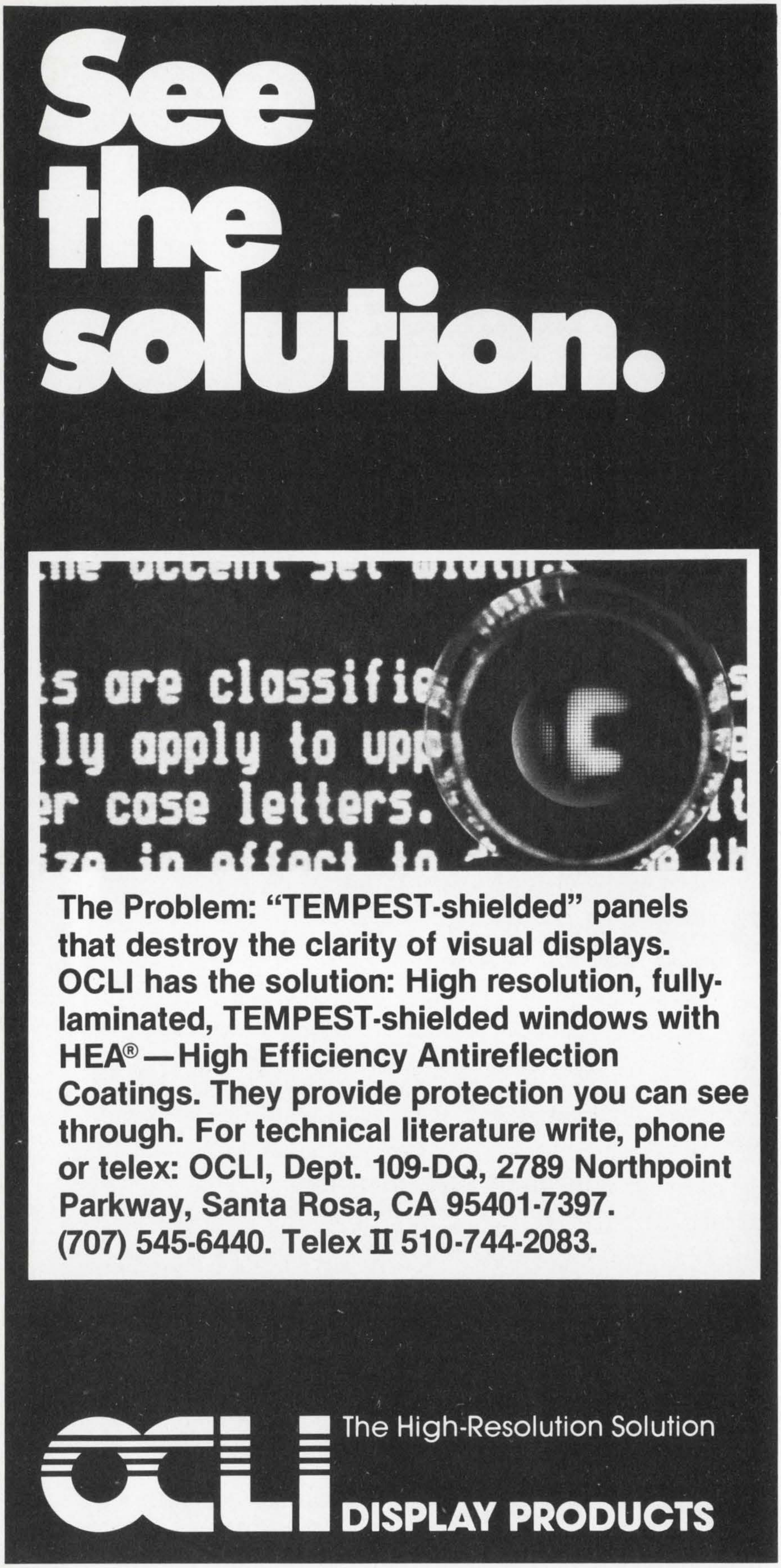

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	12	180	180	—	—	120
	12.5	—	—	150	150	—
	13.3	200	200	—	—	—
	15	—	—	180	180	150
	16.4	—	—	200	200	164
Enhanced	10	—	—	—	—	100
Expanded Print (Double Width)		Yes	Yes	Yes	Yes	Yes
Dot Addressable Graphics (Dot/In., H/V)		60/72	60/72	75/72	75/72	72/72
Max. Line Width (In.)		8.0	13.2	8.0	13.2	13.2
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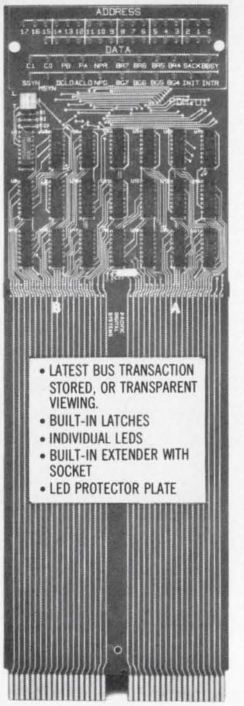

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Letters

Replete With False Assumptions

Dear Editor:

Hing-Kai Chan's article (Viewpoint, March 1982) defending foreign born engineers (FBEs) is replete with false assumptions, conclusions and ideas. He states that, with 60,000 engineering graduates a year, the small number of FBEs admitted is insignificant. Wrong. We object not only to the direct admission of FBEs but also to the large (and growing) number of foreign engineers who, after graduation from American engineering colleges, exchange their student visas for resident visas. Foreign students who graduate from American engineering colleges at the BS, MS and Ph.D. levels are, respectively, 9%, 24%, and 39%. In most cases, their education is paid for (in whole or in large part) by American taxpayers. Too many remain here by the simple expedient of obtaining a job. And since having a job is a prerequisite to remaining here, the salary is a secondary consideration.

Thus, Hing-Kai Chan's comments about the low salary for engineers are naive. Even IEEE—certainly no friend of the American working EE—was forced to admit that engineering salaries have declined, in terms of constant dollars, for the past twelve years. An important reason for this is the low salaries paid to FBEs. The fact is that, if an engineer with a masters degree and three years of specialized experience will work for $17,700 a year, then we are all threatened. Employers will adjust their salary offers accordingly.

Hing-Kai Chan is also naive when he justifies the salary offer of $17,700 a year (made in an advertisement placed by the State of Oregon's employment service) as resulting from "the recent local government's tight budget". The employer who hired this alien was not the State of Oregon, but a private company called Precision Controls, Inc. in Eugene, Oregon. The scam works like this: Before a company can hire an alien, it must first show that no American could be found to fill the job. To ensure this, they offer a very small salary—for example, $17,700 a year for a MS with three years of experience. Thus, the job is "reserved" for the alien who is waiting in the wings to grab it. To prove conclusively that no American applied for the job, the company underwrites the cost of the ad and places it in the name of the State Employment Office. State employment offices do not use low-paid engineers; unscrupulous employers do.

I was privileged to have made these and other comments to the Senate Subcommittee on Immigration on December 11, 1981.

Irwin Feerst, P.E.
Committee For Concerned EEs
Box 19
Massapequa Park, NY 11762

Find A Balance

Dear Editor:

Hing-Kai Chan's comments ("Viewpoint", March 1982) put the Foreign Born Engineer (FBE) situation into perspective. I do not want to restrict the freedom of individuals to move around the globe, but also believe in equal pay for equal work and object when an increased supply of engineers depresses my income. According to Mr. Chan's figures, we are currently "importing" over 11% of our engineers. This seems to be a rather large percentage and could affect pay scales (look what a small over-production of oil did to gasoline prices). IEEE *Spectrum* (January 1982, page 18) shows that engineers' starting salaries in constant dollars declined about 12% from 1970 to 1981. Perhaps restricting immigration would have prevented that decline, though it would also have restricted freedom.

I think the best way to achieve a reasonable balance between immigration and pay is to use a scientifically-done salary survey as the test for whether employment

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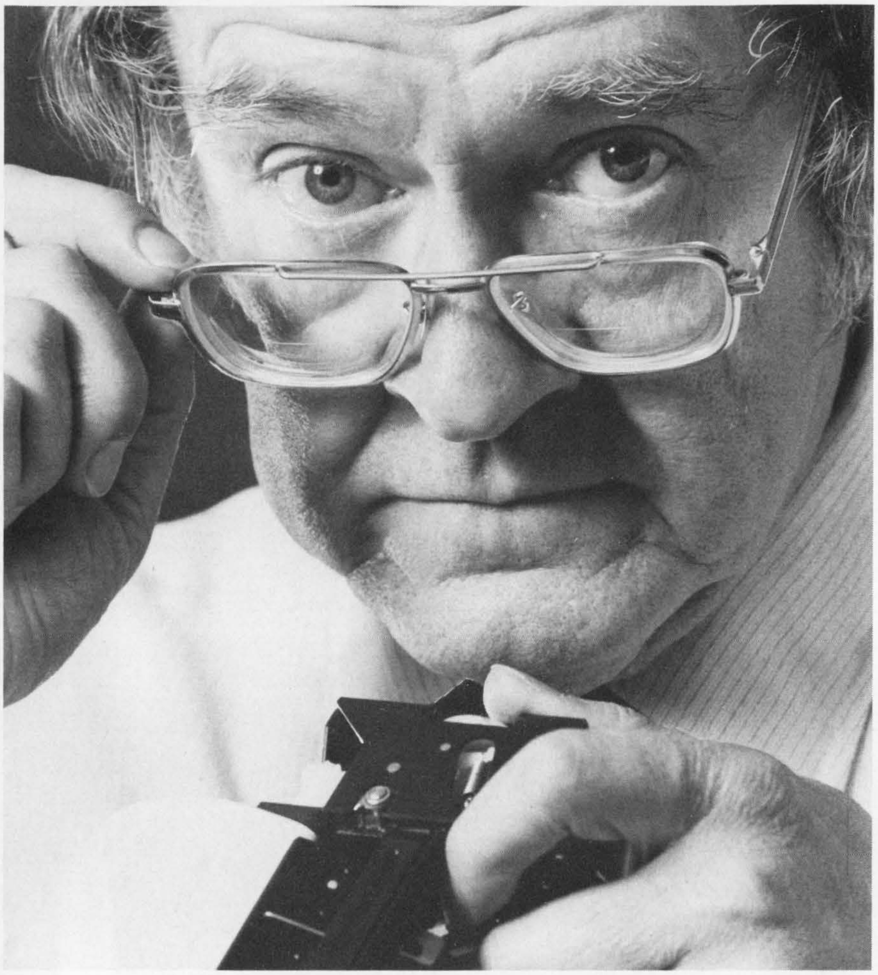

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of an FBE is to be allowed. If the salary offered is at or above, say, the median for a given field and experience level, there should be no restrictions on hiring FBEs. For EEs, the IEEE should be in a position to provide the salary survey data required.

From 1970 through 1981, BS degrees awarded in engineering increased at an annual rate of 10.7% compounded. This rate of growth can only result in a glut of engineers, not a shortage. If there ever was a shortage, it's over now and all engineers, Foreign Born or not, will have to live with the consequences.

Richard G. Wiley, Ph.D.
Senior Research Engineer
Engineering Div.
Syracuse Research Corp.
Merrill Lane
Syracuse, NY 13210

Xenophobia Strikes Again

Dear Editor:

I agree with Mr. Hing-Kai Chan in your March Viewpoint. I cannot tolerate the American engineering community speaking against foreign-born engineers. It seems to me that the fundamental wealth of a nation is its human capital. The knowledge, skills and commitment of engineers is something our country should welcome, not prohibit.

There are two other disturbing aspects to the outcry against foreign-born engineers. The first is economic: restricted entry to an occupation. This can only do harm when occupations such as medicine, engineering or others are artificially closed to newcomers. The second is plain old xenophobia. Are we jumping about and making threatening noises to those whose language or color is different? Let us live up to our ideals. We are by far the most free and generous people the world has ever known.

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Letters

PoweRotor Still Available

Dear Editor:

A letter in your February issue from Mr. Bowyer of Computer Power Products is somewhat misleading about the PoweRotor. Mr. Bowyer was a sales rep for the PoweRotor and knows that Precise Power Corp. (Bradenton, FL) bought back all manufacturing and sales activity from The Continental Group. We originally licensed this technology, which is known as the Roesel variable speed constant frequency generators and motors, to The Continental Group. They formed Continental Power Systems to produce the units, but before the project got off the ground, Continental management decided not to diversify into the machinery business. Precise Power then reacquired all rights in the technology.

Our UPS machines are still very much available for sale, and we are accepting orders. A 7½ KVA unit can be delivered from inventory at a price of $13,500. I appreciate the excellent reporting you have done about this new technology for UPS ("Flywheel UPS Produces 60 Hz At Any Speed," B. Hirshon, *Digital Design,* August, 1981). Precise Power developed and sold this patented product initially, and has had some units operating on customer computers for over four years.

The capability of providing 10 seconds of exact 60 Hz frequency with a small flywheel motor generator will be a boon to many computers for all the reasons your article discussed.

Richard T. Morash
Precise Power Corp
P.O. Box 1905
Bradenton, FL 33506

Calendar

June 1–11

Design of Integrated Circuits. Cambridge, MA. Theoretical background and experience with CAD tools and lectures on silicon compilers, signal processing systems and restructurable logic. Contact: ILP, Rm. 39-651, M.I.T., Cambridge, MA. 02139; 617-253-2691.

June 3–4

The Merger of the 80s—COLOR and the COMPUTER. Boston, MA. Also in New York June 23–24. Focus is on the art and science of effective color use in computer graphics. Contact: Educational Resources Associates Inc, 209 Harvard St, Suite 500, Brookline, MA 02146; (617)-738-8859 or 8861.

June 7–10

National Computer Conference. Houston, TX. Over 600 firms displaying the latest advances in computer hardware, software, and services. 80 technical sessions focus on the conference theme of "Professionalism," leaders of industry and government speak at plenary sessions, Professional Development Seminars probe key issues. Contact: AFIPS, PO Box 9658, Arlington, VA 22209; (703)-558-3610.

June 8–11

Hands-On Microprocessor Troubleshooting. Minneapolis, MN. Also: Washington, D.C., June 22–25; San Diego, July 13–16; Boston, July 20–23; San Diego, September 14–17; and Washington, D.C., September 21–24. Contact: Ruth Dordick, Integrated Computer Systems, 3304 Pico Blvd., Box 5339, Santa Monica, CA 90405; (213)-450-2060.

June 13–17

ICC '82—International Conference on Communications (IEEE et al.) Philadelphia, PA. Contact: Merrill W. Buckley, Jr., RCA Missile and Surface Radar, Moorestown, NJ 08057; (609)-778-2554.

June 13–17

NCGA '82, Third Annual Conference and Exposition of the National Computer Graphics Association. Anaheim, CA. Contact: NCGA, 2033 M St., N.W. Suite 330, Washington, D.C. 20036; (202)-446-5895.

June 14–16

The 19th Design Automation Conference. Las Vegas, NV. Contact: Bryan Preas, VR Information Systems, 5818 Balcones Dr, Austin, TX 78731.

June 14–16

International Robot Conference And Exhibition (Interobot). Long Beach, CA. Covered are: applications of industrial robots, CAD/CAM, flexible manufacturing systems, computer integrated manufacturing, Information and material systems for manufacturing. Contact: Tower Conference Management Co, 143 N. Hale St, Wheaton, IL 60187; 312-668-8100.

June 14–17

PRIP '82—Conference on Pattern Recognition and Image Processing. Anaheim, CA. Contact: PRIP, PO Box 639, Silver Spring, MD 20901; (301)-589-3386.

June 14–18

Eurocon '82—The Fifth European Conference on Electrotechnics (IEEE et al.) Copenhagen, Denmark. Contact: DIEU, Danish Engineers' Post Graduate Institute, The Technical University of Denmark, Bldg. 208, DK—2800 Lyngby, Denmark.

June 15–18

Microprocessor Software, Hardware And Interfacing. Philadelphia, PA. Also: Boston, June 22–25; Washington, D.C., July 13–16; San Francisco, July 20–23; and San Diego, September 21–24. Contact: Ruth Dordick, Integrated Computer Systems, 3304 Pico Blvd., Box 5339, Santa Monica, CA 90405; (213)-450-2060.

June 21–23

Bit-Slice Design Techniques. Los Angeles, CA. Intermediate level architecture and microprogramming course with hands-on practice on a 16-bit machine. Contact: Step Engineering, P.O. Box 61166, Sunnyvale, CA 94088; 800-538-1750.

June 21–23

VLSI Design. Palo Alto, CA. Contact: Hellman Associates, 299 California Ave, Dept. R, Palo Alto, CA 94306; (415)-328-4091.

June 21–25

IEEE International Symposium on Information Theory. Les Arcs, France. Contact: Prof. Carl W. Helstrom, Dept. of Electrical Engineering and Computer Science, C0014, University of California, San Diego, La Jolla, CA 92093; (714)-452-3816.

June 21–25

Digital Signal Processing: Hardware, Software, and Systems Design. Cambridge, MA. Contact: Institute for Advanced Professional Studies, 55 Wheeler St, Cambridge, MA 02138; (617)-497-2075.

June 22–24

FTCS-12, 1982 International Symposium on Fault-Tolerant Computing. Santa Monica, CA. Contact: David A. Rennels, UCLA, 3743 Boelter Hall, Los Angeles, CA 90024; (213)-825-2660.

June 29–July 1

Spectrum of Solutions '82 Exhibition. Chicago, IL. Presents a wide range of business, engineering and manufacturing applications through demonstrations, seminars and workshops by industry leaders. Contact: Prime Computer, Inc., Spectrum of Solutions '82, Prime Park, MS 15–60, Natick, MA 01760; (617)-655-8000.

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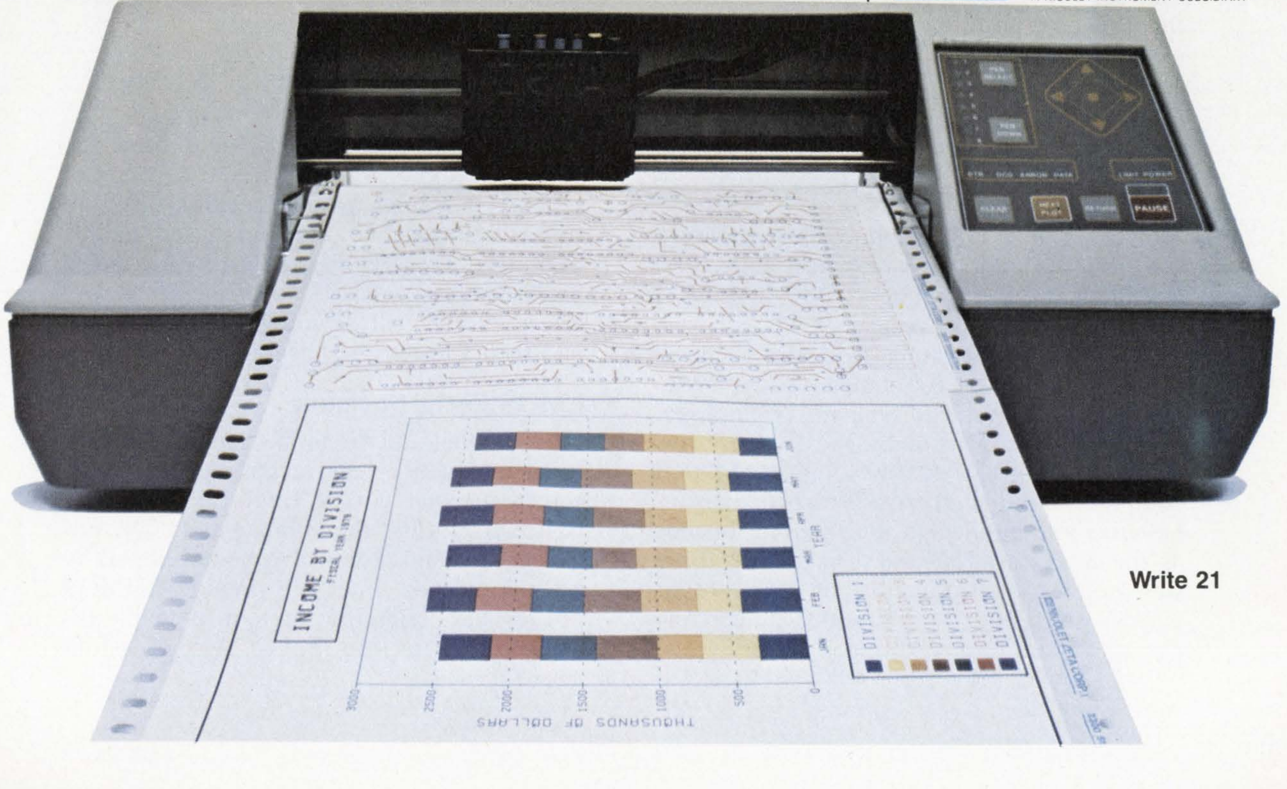


Write 21

News Update

Licensing Agreement Links Industry Giants

Data General and Standard Microsystems Corp. have signed a comprehensive, nonexclusive, world-wide patent/technology licensing agreement which will enable DG to make, use and to sell high-speed, high-density MOS VSLI circuits which will be manufactured through the use of SMC's recently-announced Titanium-Disilicide-Gate technology.

Honeywell's Earnings Down

Honeywell has announced that its first quarter computer revenues were below expectations with a significant adverse effect on the company's first quarter earnings. The revenue short fall will result from lower-than-expected computer shipments in the first quarter. Domestic computer orders are also running below year-earlier levels. The company reported that its control systems business is meeting its order, revenue and earnings plan for the quarter. The company also announced that it has discontinued the use of the equity method of accounting for its investment in Cii-Honeywell Bull effective January 1, 1982. This change was necessary because, in management's opinion, due to the French government nationalization of the French-controlling interests in Cii-Honeywell Bull, Honeywell no longer exercises significant influence over the operating and financial policies of the company.

Seagate Co-Founder Starts Own Disk Drive Firm

Slated for mid-1982 product introductions, SyQuest Technology, a new firm started by Syed Iftikar, will manufacture low-cost OEM fixed and removable Winchester disk drives. Prior to his establishing SyQuest Technology, Iftikar was co-founder and VP/Mechanical Engineering at Seagate Technology. The immediate goal of SyQuest is to introduce storage devices (the SQ-series) that computer manufacturers will recognize as innovative and applied to their memory needs as the Seagate ST506 5-¼″ fixed disk drive was upon its introduction in 1980. "Our aim," says Iftikar, "is to produce a data storage equivalent of a VW Bug."

Plessey Dial-In Design Service

Plessey Semiconductors UK has started a bureau service to enable customers to do semicustom design from their own office using Microcell or CMOS gate arrays. A designer can use the bureau service for all logic simulation including dynamic performance and to check that his re-constructed logic agrees with the original simulation. Time is charged according to the terminal hours connected and the amount of central processor time used. Batch facilities are available at reduced rates and the service is available 24 hours a day.

Ford Plans To Build Chips

A Ford Motor Company affiliate is to build an IC design center near Colorado Springs, CO. The 25,000-square-foot facility will be headquarters for Ford Microelectronics, a newly formed subsidiary of Ford Aerospace & Communications Corp., which will design advanced ICs for both aerospace and automotive use.

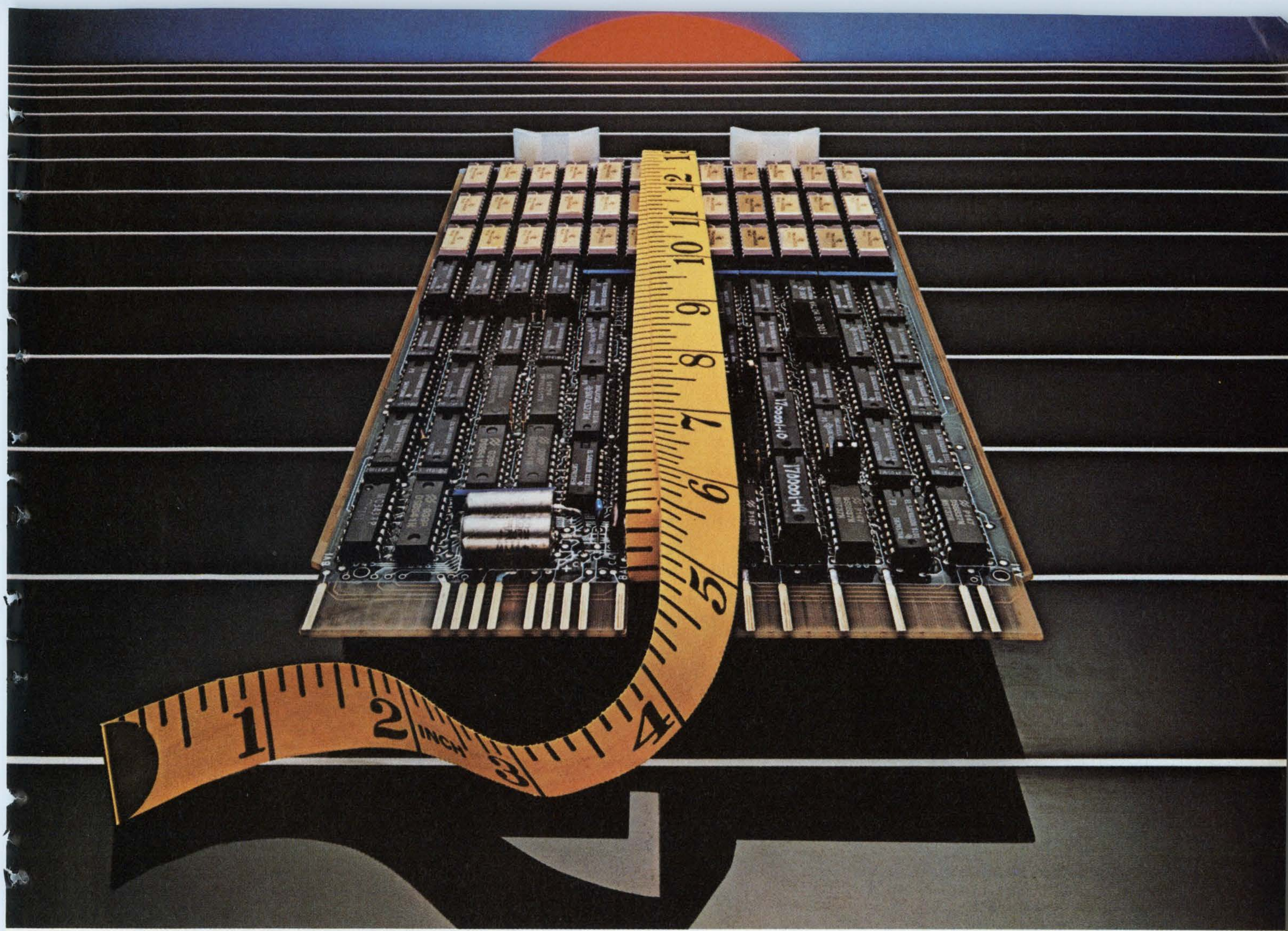
The Ford Microelectronics organization will consist of computer-aided design (CAD) and IC designers, along with support personnel, from the semiconductor industry and universities. Circuits designed by the new subsidiary will be produced by outside semiconductor manufacturers.

Century Data and Nestar Sign $1.5m Contract

Century Data Systems has announced the signing of a $1.5 million renewal contract to provide Marksman Winchester disk drives to Nestar Systems. The units purchased include Century's 190MB and 380MB Advanced Marksman series (AMS) of Winchester disk drives. Nestar will be integrating the drives into their Cluster/One local network.

CMOS Fever Spreads

Intel, Intersil and General Electric have entered into a five-year technology exchange agreement that covers Intel's high density CHMOS process, the company's 80C51 single-chip μC and products to be developed by Intersil and GE. Intel will provide CHMOS process and design information to enable Intersil to manufacture the 80C51 and custom



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It also provides 22-bit addressing capability. High-density 128 KB and 256 KB capacity on a single "dual" board. And address space DIP selectable from 256 KB to 4 MB.

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PDP-11*	TMM20000[2]			X	X	X
VAX*	TMM30000				X	X
Multibus†	TMM40010A[2]	X	X	X	X	

[1] Parity optional

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products designed by GE for the CHMOS process, and Intel will receive design information needed to manufacture Intersil and GE-designed standard and custom products built on the CHMOS process or derived from the 80C51 architecture.

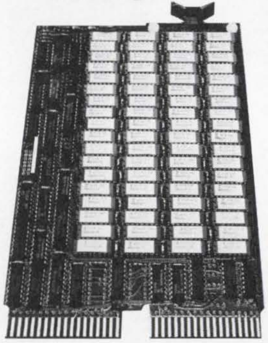
Data Electronics to Make Tape Cartridge

Data Electronics, Inc. (DEI) and 3M Corp have announced that DEI has been granted a license to manufacture and market the ANSI ¼" digital tape cartridge in both its 300 and 450 foot versions. Data Electronics is adding this to its line of ¼" digital cartridge tape drives to meet increasing customer needs of DEI drives for Winchester disk back-up. "This license," says Hal Georgens, DEI Chairman of the Board, "will allow efficient integration of future cartridge enhancements and forthcoming tape drive developments."

CP/M For The 68000 Expected This Year

Digital Research has announced that it has agreed with Hitachi to develop Digital Research's CP/M operating system and several application languages for the 68000 μP. Digital Research believes that CP/M-68K will become a standard operating system for 68000-based μCs and that the agreement will speed up the availability of CP/M-68K. Digital Research and Hitachi also expect to develop Pascal/MT+ for the 68000. Hitachi's SPL/H 68000 systems implementation language and its ANSI standard FORTRAN compiler also will be transported to CP/M-68K to complete the line of languages supporting the 68000. It is expected that both CP/M-68K and Pascal-68K will be completed in June and will be available in the third quarter of this year. CP/M is the most popular operating system used in personal computers.

MicroSTOR–1123



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IBM Develops Denser, Faster, Lower-Power Bipolar RAMs

IBM engineers have successfully combined three circuit design techniques in an experiment that could produce 100% denser, 25% faster and 30% lower power bipolar arrays than any used today.

These techniques, disclosed at Compcon Spring/82 in San Francisco, can be applied to many types of bipolar memory chips. Used in an SRAM, the techniques can produce a 2K × 10 array on a chip smaller than 6×6 mm^2. The typical access of this array is predicted to be 15 ns with a 1.8W power dissipation.

Engineers started the experiment with a 1K × 10 static RAM having a 20ns access time, a 22ns write time and dissipating 2.2W on a 5.3×5.3 mm^2 chip. The objective was to reduce access and write times by 25%, reduce power dissipation by 30%, and double the density on a chip measuring less than 6×6 mm^2. Engineers used a complementary transistor switch (CTS) cell in the experiment.

The circuit design techniques used in the array experiment approach speed, power and density through word line selection, writing and sensing.

The engineers, from IBM (East Fishkill, NY) took advantage of CTS density by physically matching the peripheral circuitry with the pitch of the array. This entailed combining the read and write circuitry typically found in arrays. The resulting circuits perform both read and write functions, saving space and power.

The engineers employed a transient selection scheme to reduce power dissipation even further. Power is needed most when the array is being selected; power requirements are far lower following selection. The transient power is self-regulating. The high transient current used during selection to enhance speed is reduced significantly to a steady state select current when selection is complete.

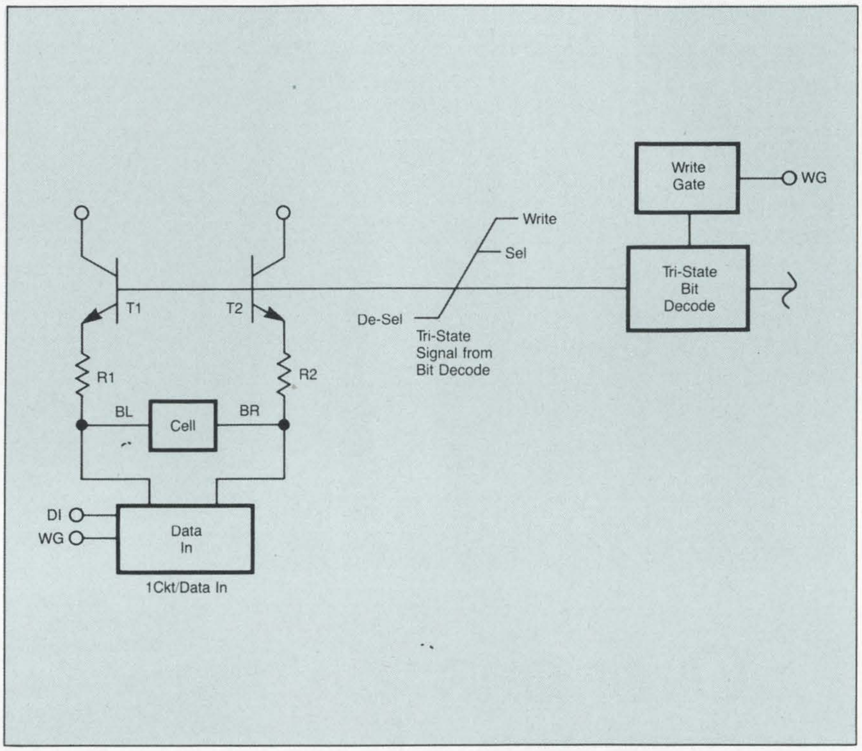


Figure 1: Significant improvements in power and density in bipolar VLSI RAM arrays have been achieved by IBM. A tri-state bit selection/write technique is illustrated here. The write function and bit decode circuitry were combined to give the decode driver both bit selection and writing capability.

The large selection voltage swing (1.5 V) provides enough voltage separation between selected and unselected cells to ensure no cell interaction.

The final technique involves the sensing scheme in the array. IBM engineers have isolated the high-bit-line capacitance from the switching input nodes of the differential sensing amplifier. This isolation results in higher performance. Sensing is accomplished with two integrated transistor/Schottky diode devices and two load resistors.

Attributes of the design techniques include:

- Word Line Selection. Self-regulated current source to ensure a low drain line, steady state current. The high transient current used for selection is reduced to a much lower steady state select current until another word line is selected. Voltage swings wide enough to guarantee no cell interaction between selected and unselected cells. This large voltage swing does not impact performance because transient current drive is used for select and active pull-up is used for de-select.
- Writing. Write function combined with bit decode circuitry to give the decode driver both bit selection and writing capabilities. This is done with a tri-state bit line driver scheme. The result is significant reduction in chip power dissipation and silicon area.
- Sensing. Sensing scheme isolates the high bit line capacitance from the switching node of the differential amplifier inputs, resulting in improved sensing speed.
- Predicted Experimental Array Results. 2K × 10 RAM in a 6×6 mm^2 chip using complementary transistor switch cells. Array has typical access of 8 ns using 1.5 W.

HMOS-III Technology Improves Semiconductor Density And Performance

HMOS-III represents a further downward scaling of the HMOS process introduced by Intel in 1977, and improved with HMOS-II in 1979. The benefits of HMOS-III can be noted via the development, as a demonstration vehicle, of a 1K x 4 bit static RAM. Using conservative design techniques, this 4K static RAM, with a 15-ns access time, occupies an area of 13,650 square mils. It has a memory cell size of 0.98 mil^2 (20μ x 31.75μ).

The demonstration RAM operates from a single 5-V power supply with common input/output; all parts are TTL-compatible.

In addition to the 15-ns access time (current products show 45-ns maximum access times), the device features automatic power-down and low power consumption. Active power consumption is 100 mA, while standby power is only 20 mA (maximum).

A comparison of the demonstration 4K static RAM with other HMOS and HMOS-II products of similar organization is shown in **Table 1.**

	Intel 2148 1K x 4-bit static RAM	Intel 2148H 1K x 4-bit static RAM	Intel HMOS-III Development vehicle 1K x 4-bit static RAM
Technology	HMOS	HMOS-II	HMOS-III
Year of introduction	1979	1980	n/a
Address access time (ns)	70	45	14
Chip select address time (ns)	70	45	21
Organization	1K x 4	1K x 4	1K x 4
Automatic power-down	yes	yes	yes
Common I/O	yes	yes	yes
TTL compatible	yes	yes	yes
Active power	140 mA	180 mA	100 mA
Standby power	300 mA	30 mA	20 mA
Power supply	+5V only, ±5%	+5V only, ±10%	+5V only, ±10%

Table 1: Comparison of HMOS, HMOS-II and HMOS-III 1K x 4-bit static RAMs.

A New Array Of Arrays

Texas Instruments and Motorola are offering some new developments to watch in LSI Gate Array design. The basic idea of building chip arrays consisting of hundreds or thousands of individual gates has been around for over a decade. Arrays have always offered a lower cost method of producing custom ICs than was possible with a fully dedicated custom design. Other advantages include higher levels of integration, lower power, less board space and higher performance compared to producing the same design in SSI or MSI circuits.

But all of these advantages are well known by now; the really new additions from TI and Motorola are CAD assistance. No longer is the user required to interconnect as many gates as he can to produce a dedicated functional chip; the CAD being offered by both companies does most of this work.

Two Design Approaches

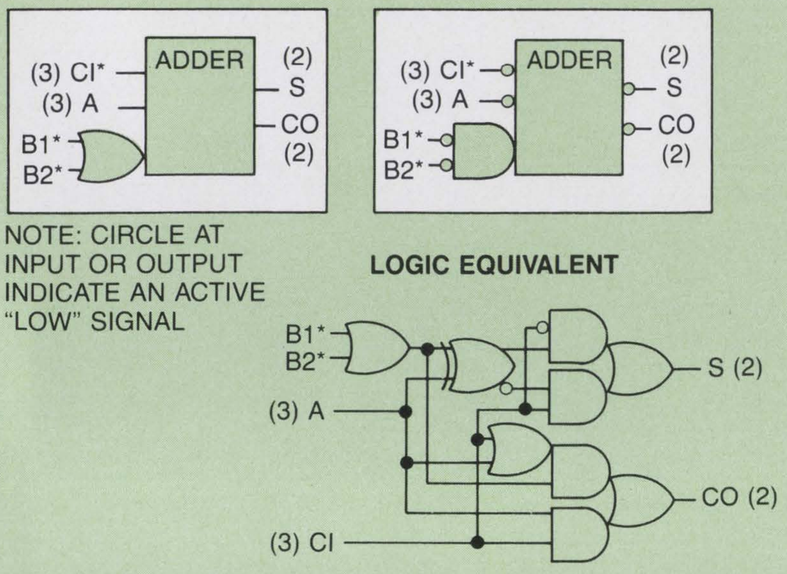
Comparing the two approaches may be easier than either company indicates in its published literature. The user's task is now to define his basic logic functions. Not in terms of gates, but in terms of full functional logic elements such as adders and flip-flops.

Motorola's approach allows the user to define his logic in predetermined (and preconnected logic elements). These logic functions are cataloged and characterized just like their SSI/MSI counterparts. **(Figure 1).** Product manager John Carey compares the design task of a Motorola Macrocell Array with producing the same design using a double sided PCB and SSI/MSI discrete IC packages. The user selects the functions needed; the CAD program places the selected functions into the cells on the array. The individual hardwired cells/functions are then interconnected in a unique single level metal interconnect scheme.

Motorola has about 100 standard Macrocells in its library and will probably be adding more. They claim that it is possible to use 100% of the array in some cases; however, most designs average 90% utilization of the array cells. All of the Macrocell arrays being offered by Motorola are ECL arrays, but two are fully compatible with Advanced Low Power Schottky TTL.

Motorola's method of designating the Macrocell Arrays can be a bit confusing. For example, the MAC1200 ECL Macrocell array is equivalent to 1192 gates if full adders and latches are used in the cells; if flip-flops and latches are used, the equivalent gate count on the array drops to 904. To muddy things even more, the array is defined as having a total of 106 cells of which 48 are major, 32 are interface and 26 are

M50—FULL ADDER



TRUTH TABLE

A	B1	B2	CI	S	CO
L	L	L	L	L	L
L	L	L	H	H	L
L	H	X	L	H	L
L	X	H	L	H	L
L	H	X	H	L	H
L	X	H	H	L	H
H	L	L	L	H	L
H	L	L	H	L	H
H	H	X	L	L	H
H	X	H	L	L	H
H	H	X	H	H	H
H	X	H	H	H	H

tpd (A, CI → S) = 1.35ns
tpd (A → CO) = 1.2ns
tpd (B1, B2 → S) = 1.7ns
tpd (B1, B2, CI → CO) = 1.35ns
PD = 26mW

Figure 1: This Full-Adder circuit is typical of the Motorola Macrocells. The designer selects logic functions like this adder from a catalog. The data provided resembles the information presented for a discrete full adder MECC 10,000 IC. By selecting functions like this, the gate array, in this case Macrocell array, can be tailored to perform many complex logic functions.

output.

The confusion is not as great as it appears when you consider how much logic you can pack into those 106 cells. If John Carey is correct about the design being as easy as double sided PCBs, then it should have broad appeal to designers now using that method.

Texas Instruments promotes its products as gate arrays, claiming that 80% of each array can be fully utilized. TI's method is equally difficult to understand until you discover that their basic approach is quite similar to Motorola's. TI, however, defines the logic cell functions in CAD software rather than prewired/predefined logic cells **(Figure 2)**. TI currently has 70 predefined functions available. This approach can permit greater interconnect flexibility when the gates are interconnected with 2 levels of metal interconnects. It means, however, that the individual functions may never be connected in exactly the same way in each array design.

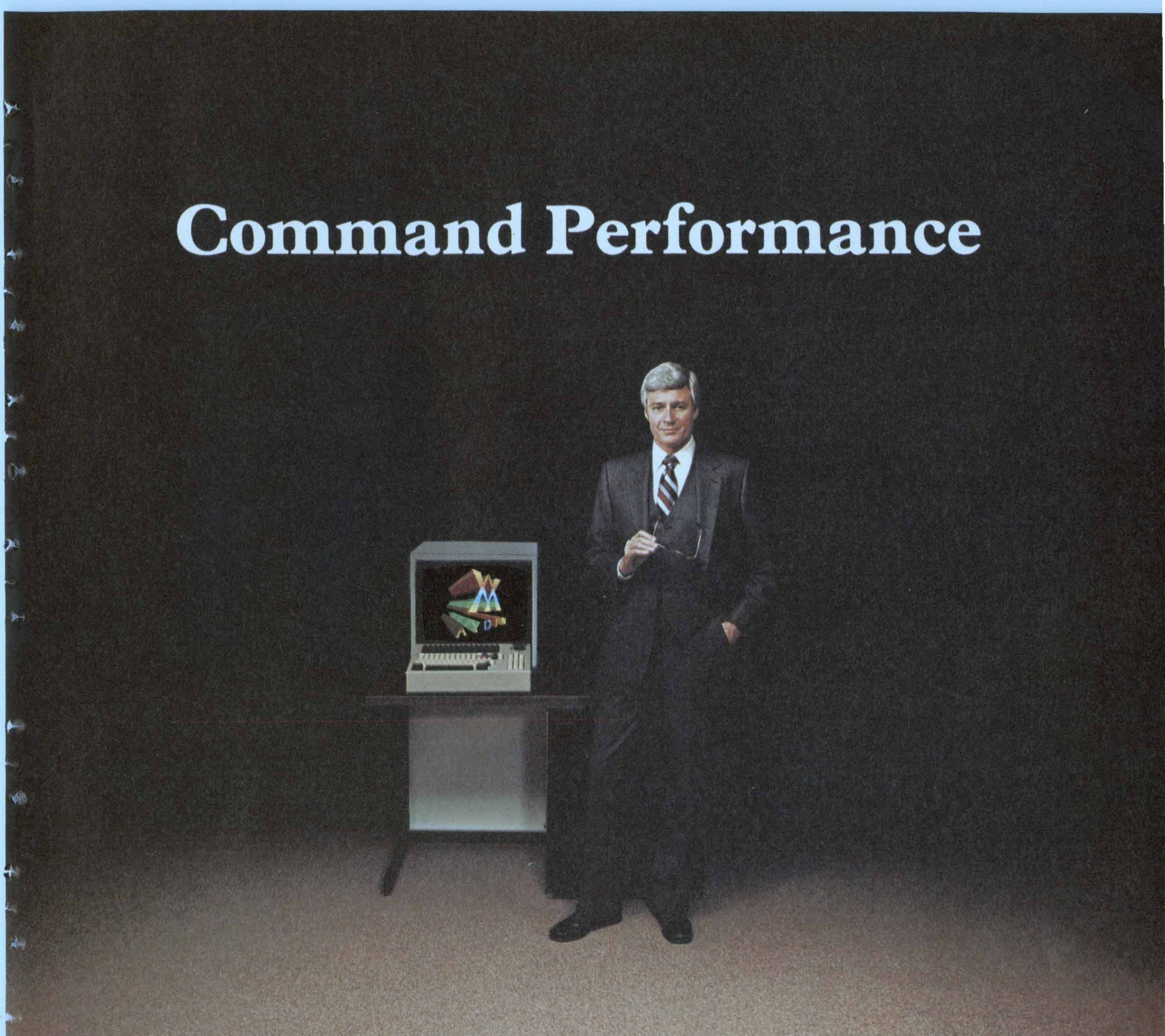
TI defines its standard functions in CAD software; the major difference with Motorola's approach is that the functions are not characterized and defined as well. In reality, while both TI and Motorola are capable of producing very similar finished products, they offer different levels of performance.

Choosing An Approach

The real choice rests with the designer. He should not only pick a technology that will meet his performance needs, but select a CAD approach he feels comfortable in using. Since many companies offer gate array products, the designer considering a gate array approach should shop for CAD first. Responsibility for the ultimate performance of any design rests with the designer. Obviously, if you are selecting a gate array you will have a lot at stake in its operation. If you are not comfortable in the design phase, you are prone to make mistakes.

The basic decision to develop an array should be the first consideration. What will it add to your product that you are not able to get by any other approach? Will it reduce your product cost, improve performance, make it difficult for your competition to copy your approach? These and many more basic questions should be answered before you approach an array manufacturer. Once you are sure that a gate array will solve your problems, then seek a design approach you can comprehend without going through an extensive learning process.

Both TI and Motorola offer design assistance via regional design centers around the country. After you have carefully examined all of the CAD approaches you will be ready to make better choices. The next obvious question is what kinds of arrays are available to pick from.



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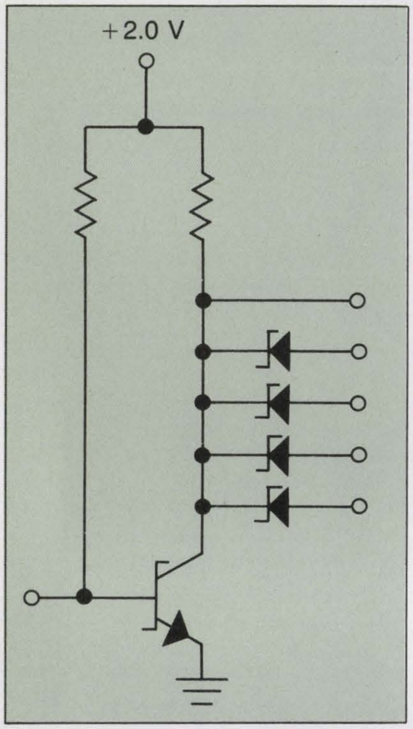

Figure 2: Texas Instruments produces its arrays using this basic internal gate configuration. The CAD program must then define the logic functional element as well as the most efficient interconnect arrangement on the array.

TI's family of arrays is limited to Advanced Low Power Schottky TTL, while Motorola currently offers both ECL and ALP/STTL arrays with CMOS and MECL to be added within the next year or so. **Table 1** indicates some of the available arrays from both companies, but is far from a complete list of available products. Many other semiconductor companies offer arrays—each with different features.

Costs do not always tell a true story. TI for example has a front end cost of about $40,000. Motorola quotes prices in the range from $16,000 to $29,000 that includes delivery of 10 prototypes, 100% tested. In both cases, volume production costs are separate. The buyer should be aware of all costs involved in developing an array. Volume production will not always make up for high development costs.

—Groves

MOTOROLA-MACROCELL-ARRAYS

PARAMETER	MCA 1200 ECL	MCA 600 ECL	MCA 500 ALS
• **Maximum equivalent gates**	1192	652	533
• **Major macrocells**	48	24	24
• **Interface/Input macrocells**	32	25	26
• **Output macrocells**	26	18	24
• **Maximum gate delay**	1.2 ns	1.2 ns	4.0 ns
• **Power dissipation**	4 W	2.5 W	1.1 W
• **I/O interface**	MECL 10,000	MECL 10,000	ALS TTL
• **Design interface**	CAD	CAD	CAD

These arrays are currently available from Motorola. During 1982 they will be introducing several new array products in ALS-TTL and ECL with complexities up to 2800 gates. In 1983 Motorola is expected to add MECL 10K and CMOS arrays.

TEXAS INSTRUMENTS

ARRAY TYPE		**TAT010**	**TAT020**
TOTAL GATE COUNT		1260	2420
USABLE GATE COUNT		1000	2000
INPUT CONNECTIONS	STD	88	120
	ECL XLATOR	6	6
OUTPUT CONNECTIONS	STD	44	60
	HI DRIVE	24	32
	ECL XLATOR	6	6
POWER SUPPLIES	5V	2	2
	2V	2	2
	0V	4	4
INTERNAL GATES—	SPEED ns (typ)		1.0
	POWER μW (typ)		300
INPUT BUFFERS—	SPEED ns (typ)		1.0
	POWER mW (typ)		4.0
OUTPUT BUFFERS—	SPEED ns (typ)		4.0
	POWER mW (typ)		10.0
TOTAL ARRAY POWER W	(max)	1.5	2.5
TECHNOLOGY		ALS/TTL	

Table 1: Comparison chart of some of the arrays available from Texas Instruments and Motorola. While both companies can produce similar finished products, they offer different levels of performance.

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CAD/CAM Revenues Exceed $1 Billion

Last year's revenues for the CAD/CAM industry exceeded $1 billion, according to Dr. Gauhan, Vice President and Director of Dataquest's CAD/CAM Service.

Dr. Gauhan added that the $1 billion figure includes revenues for turnkey CAD/CAM companies; sales of CAD/CAM products by computer companies, such as IBM and DEC, and sales of CAD/CAM software packages designed to run on general-purpose computers.

Turnkey revenues alone reached $682 million in 1981 — a 40% annual growth rate from the $484 million of 1980. "While growth of that magnitude would be quite impressive for some industries," Gauhan observed, "it is a sharp drop from the 60% plus growth that we have seen in the CAD/CAM industry for the past several years. There is still enough latent demand out there to sustain the growth rate of previous years, but the industry definitely has felt the impact of high interest rates and a slackening of investment in capital equipment."

Another significant trend in the CAD/CAM industry is a shift in market share among the major vendors. Dataquest estimates that Computervision, the leading turnkey company, maintained its 40% market share. Calma, which was acquired by General Electric in 1981, gained 2% points and now has 15% of the turnkey market, while Applicon and Integraph each hold a 13% share.

"General Electric has already made itself felt in this industry," Gauhan noted, "and Calma has established itself as the number two turnkey vendor. Now that Schlumberger's board of directors has approved the purchase of Applicon, 1982 will be a very interesting year in the CAD/CAM industry. We will see the giants, General Electric and Schlumberger, battling for market share with Computervision, the recognized industry leader."

Gauhan pointed out that in 1981 computer companies became increasingly important in the CAD/CAM marketplace, and he expects that trend to continue. IBM, DEC, Prime Computer, and Perkin-Elmer all made major efforts in the CAD/CAM arena last year. Gauhan forecasts that virtually every major computer company will become active in selling directly to the CAD/CAM market in the future.

He also observed that growth in the IC design segment of the CAD/CAM market was relatively flat in 1981. Dataquest estimates that revenues in this area grew at less than 20%, compared to the 40% growth in the turnkey industry as a whole.

DEC Inks Agreements With 6 CAD/CAM Software Houses

Software products spanning a range of electrical and mechanical CAD/CAM applications, including µP software development, IC design, PCB design, gate array design and mechanical design, will be cooperatively marketed by DEC and six software companies. Both DEC and the individual software firms will configure the complete hardware/software systems to meet specific applications based on DEC's family of VAX–11 µCs. All of the programs can be run on the VAX–11/780 and VAX–11/750 minicomputers.

Program packages are as follows:

- *Mechanical CAD.* Auto-Trol Technology is offering new 3D CAD/CAM software systems for interactive engineering design, modeling, analysis, and numerical control (NC) capabilities, plus flat pattern development and nesting, finite-element modeling, and links to finite element analysis. The software systems can be used in engineering manufacturing applications.
- *µP Software Development.* Boston System Office, Inc. offers software development tools that convert any VAX–11 system into a µP development system for practically all available µPs. The software systems include a line of µP development systems supporting from one to over 100 users. They encompass software development tools for more than 30 families of µPs.

Development tools include relocatable macro assemblers, cross-reference programs, high-speed linkers, subroutine librarians, object format conversion routines, software interfaces to emulators and PROM debuggers and PASCAL cross-compilers. They enable users to rapidly develop and debug software for different µPs on the same computer system.

- *Logic Simulation.* Comsat General Integrated Systems is offering three CAD/CAM software packages — TEGAS, LOGIX, and SUPER–COMPACT. TEGAS is a logic simulation and test generation package for LSI and VLSI ICs. Its functions include logic verification, design verification, fault simulation, and automatic test pattern generation. Uses include generation of production and diagnostic tests for digital systems, worst case timing analysis, race and hazard analysis, and assessment of diagnostic and production test effectiveness.

DEC will work with each software house to produce complete systems for CAD applications.

LOGIX is a schematic design capture system that generates and maintains information common to engineering, drafting, and manufacturing of digital electronic circuits. It is often used in conjunction with TEGAS.

SUPER–COMPACT, an analysis, optimization, and synthesis program for microwave design, replaces the COMPACT program. New features include interactive graphics; transmission line synthesis; 1, 2, 3, and 4-part circuit capability, and enhanced optimization techniques.

- *Geometrical Modeling and Simulation.* EUCLID, an integrated CAD/CAM system including a solid-geometry modeling package developed by Matra-Datavision, enables users to generate and manipulate computer representations of simple or complex shaped parts. A model created with EUCLID has the coded properties of the real solid object it represents. Such a model can be used in design, kinematic analysis, generation of dimensioned drawings, numerical control tapes, and additional object-specific documentation.

EUCLID enables users to define and transform geometric elements, construct 2D/3D elements, and perform topological transformations on them such as sectioning, fusing, defining common elements, and removing undesired elements. The package can be used in a variety of application areas including general mechanical, design, drafting, numerical control programming, architecture, kinematic analysis, landscape design, and hydrodynamic analysis.

- *IC Layout Verification.* NCA Corporation is offering ERC, DRC, MDP, and NCC software packages for IC layout verification. ERC detects many types of design and digitizing errors such as missing contacts, missing transistors, internal shorts, switched connections, transistors that cannot be driven high or low, and signals with no fanout. The package checks for consistent use of text labels digitized within a chip as well as on bonding pads. It checks that all bonding pads with the same name are connected together and that none with different names are shorted. Input to ERC is from industry standard graphics systems or pattern generators. Technologies supported include bipolar N-channel silicon gate, P-channel metal gate, CMOS, and SOS. Error output is cell oriented. For each error, the output includes all nodes and devices involved in all layers for that error. ERC can also check for electrical node continuity within a chip.

The cooperative approach should ease CAD/CAM system design for users of VAX-11 minis by reducing the problems of finding or creating software.

DRC automatically identifies design rule violations in ICs. It also generates logical combinations of layers. The software, which is technology independent, is generally accepted as the industry standard. Its logical operations are inclusive and exclusive OR, AND, and ANDNOT. Design rule checks are internal, external, and enclosure. The programs accept input data on magnetic tape from most industry standard graphics systems and pattern generators. Error output is generated in plottable form.

NCC is a software package that compares an electronic circuit to its representation in a schematic. It automatically detects discrepancies between the two and reports them to the user. Electrical Parameter Check analyzes a proposed circuit to provide information for loading and speed analysis. It measures device sizes, signal capacitance, and other electrical parameters. It can generate output to analog and logic simulators.

Mask Data Preparation (MDP) is a program that enables a computer to take the results of its IC design process and transform the information so that it can be transmitted to equipment that actually generates mask patterns used in manufacturing.

- *Electronic Gate-Array Design.* Silvar-Lisco is offering CAD/CAM packages suitable for electronic engineering applications, including EDA-GARDS. EDA-GARDS is a gate-array layout system providing interactive and fully automatic placement and routing capabilities to designers. The software package can handle a variety of semiconductor technologies, including CMOS, ECL, TTL, and I^2L. Routing capabilities encompass both single- and two-layer metal gate arrays. EDA-GARDS maintains design rules throughout the layout process, and software interfaces are available to a variety of graphics editing systems. A related supporting CAD/CAM system, EDA-SDS, is a schematic and netlist processing system. The software enables users to develop schematics interactively, and it can extract netlists automatically.

EDA-SDS supports hierarchical netlists and schematics, enabling designers to describe a circuit in a top-down fashion, using abstraction levels. The software enables a user to expand a hierarchical description into a gate-level description for later use by layout or simulation systems. EDA-SDS also supports interactive partitioning of netlists. Interfaces to a variety of other CAD software, including EDA-GARDS and CAL-MP, are available.

This cooperative marketing approach should aid users of VAX-11 minis by making it possible to acquire software support from DEC. It can greatly reduce the problems of finding or creating software for the expanding CAD/CAM applications being developed throughout all industries. Probably the most significant advance is the area of mechanical design of solid structures.

—Groves

Full-Duplex Communication Over A Single Wire

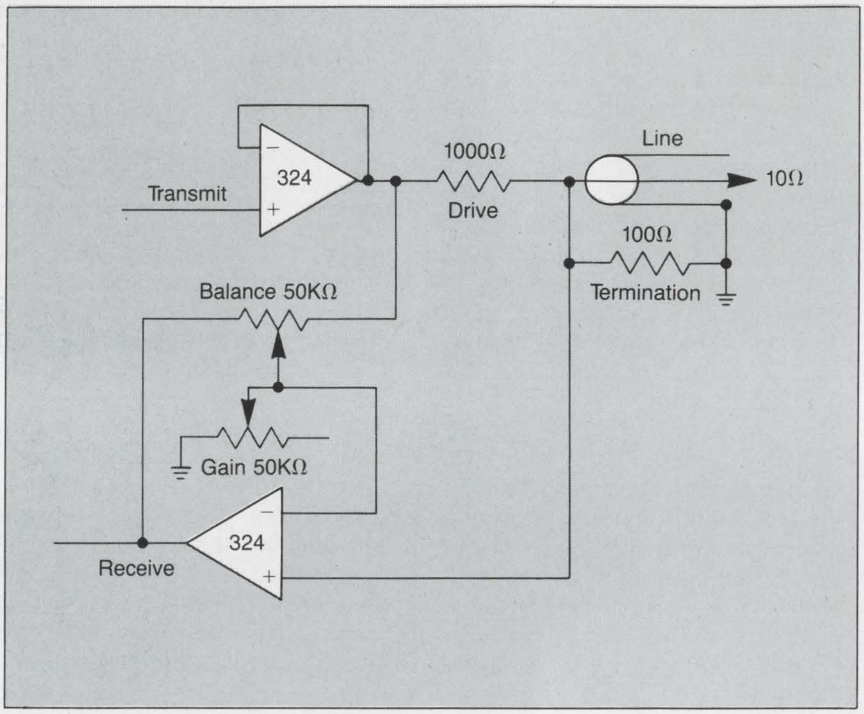

Figure 1: Full-duplex communication over a single wire can be achieved with the circuit shown using two quad 324 op amps and four resistors.

The scheme detailed in John Meng's article, "Bi-Directional Handshaking Over a Single Wire" *(Digital Design,* December 1979) suggested a more general approach allowing even independent analog voltages to be exchanged across a line simultaneously.

The method employed makes use of the fact that, if a resistance is placed between a common line and the driver at each end, the line voltage will be the average of that present at the drivers' outputs. All that is necessary to determine the voltage being received, in this case, is to subtract half the transmitted voltage from the line voltage and double the result, a task ideally suited to an operational amplifier. In fact, this function is complicated somewhat by such conditions as wire conductance and termination resistors to extend frequency and distance ranges.

Figure 1 may be viewed as using the following approach: the potentiometer network duplicates the transmission line, including wire impedance and terminations as well as the drive resistors described previously. If no line termination resistors are required for the particular application, the potentiometer to ground (marked 'gain') is eliminated. When properly adjusted, the V-input to the receive op amp equals the voltage on the line when the output of the receive op amp equals that actually being transmitted by the other side, thus balancing the op amp. The transmit op amp merely buffers the transmit signal, providing unity gain.

Once assembled, the system may be easily calibrated if no line terminating resistors are used; the drivers are set to different (known) voltages, and each balance potentiometer is set so that the signal received from each end equals that transmitted from the other. Isolation can be verified by varying the transmitted voltage at one end and observing that the received voltage is not altered; this technique also allows the circuit to be balanced if the opposing transmit voltage is unknown, but constant.

If line termination resistances are necessary, calibration is more tedious, and knowledge of the opposing transmit voltage is necessary; the two controls must be adjusted so that the received voltage at each end not only does not vary with that transmitted from that end, but also equals that transmitted from the other end. This may be accomplished by repetitively setting the balance control to eliminate receiver variance, followed by adjustment of gain for correct received voltage.

If line amplification is desired, a repeater can be constructed by combining two circuits "back-to-back," with one side's receiver becoming the opposite side's transmitter; thus, only two op amps are required.

On the author's prototype—with a 4.7V supply, a quad 324 op amp for both transceivers, a 10Ω line with 100Ω terminations to ground on each end, 1000Ω line driver resistors, and 50KΩ potentiometers for all adjustments (which revealed the need for a smaller value for the sensitive gain control)—the circuit passed values from 0.2 to 3.2 V with less than 10 mV interference from the opposite channel. Total current used on both ends varied from 2 to 10 mA, depending on transmitted signal.

Charles Green, Mantech International, 17 Shangrila Drive, Suite 200, Lexington Park, MD 20653.

Setting Up And Recording Difficult To Capture Waveforms

Waveform recorders make it possible to record signals of interest occurring in μP-based systems. A waveform recorder will trigger based on a signal from a logic analyzer, and begin recording at this trigger, or a precise amount of time before or after the trigger occurs.

Figure 1 shows a typical setup using a logic analyzer and waveform recorder. An HP5180A waveform recorder is used with an HP1311A CRT Display in this application for viewing the recorded waveform. The logic analyzer used here, an HP1611A, has "personality modules" for connecting directly to seven major μPs. The HP1611A also has a general-purpose module available for testing circuits not controlled by one of these seven μPs. Logic analyzers with either dedicated or general-purpose connecting modules may be used in this application. Only three connections between instruments are required: 1) Send μP Instruction Address To Logic Analyzer, 2) Send Trigger Output From Logic Analyzer To Waveform Recorder/Transient Digitizer Trigger Input, and 3) Connect Input Signal To Waveform Recorder Input Channel.

Send μP Instruction Address

If a logic analyzer is to be used with a dedicated personality module for the μP in the circuit, this module needs to be attached to the μP **(Figure 2A).** When a general-purpose module or a logic analyzer with general-purpose probes is selected, the probes must be individually connected to the μPs address pins. **(Figure 2B).**

After making this connection, the μP instruction address must be selected that will initiate a trigger. This is usually done by specifying the instruction address of interest as a "trace" condition for the logic analyzer. For example, when the HP1615A Logic Analyzer is used, the beginning of the trace is selected by entering the instruction address into a trace specification "menu."

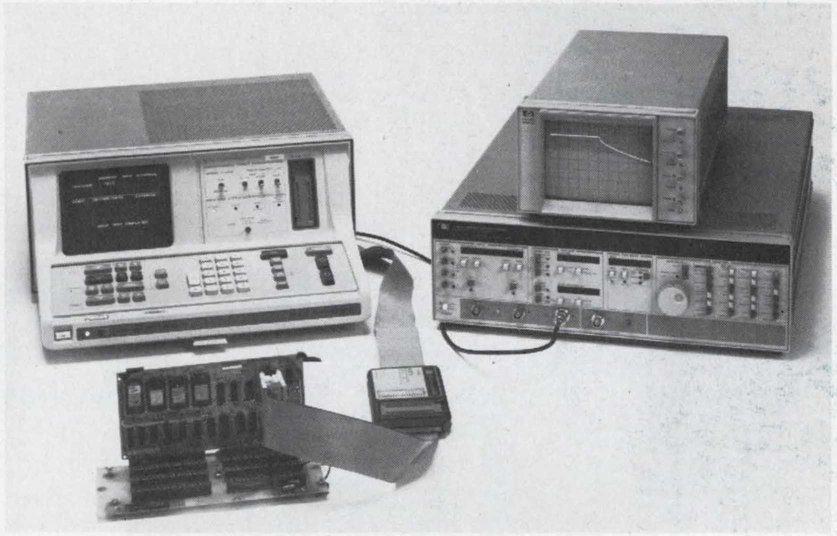

Figure 1: A typical equipment set-up using the 5180A Waveform Recorder with a HP1611A Logic Analyzer.

Send Trigger Output

When the logic analyzer receives the selected instruction address from the μP, it begins a trace. At the same time, the trigger output from the logic analyzer should be used to trigger the waveform recorder. To do this, the logic analyzer's trigger output must be connected to the external trigger input on the waveform recorder (The trigger level for the waveform recorder's external trigger input must be appropriately selected for the trigger signal your logic analyzer sends.)

Connect Input Signal

Finally, the signal of interest must be connected to an input channel on the waveform recorder. Some waveform recorders (including the HP5180A) provide selectable input voltage ranges. If the waveform recorder has this feature, the input voltage range should be specified. (The voltage range of the input channel must be appropriate for the signal that is being recorded.)

Some Examples

Using the procedure described, it is possible to record and analyze signals occurring at specific times during the μP program. For example, it may be necessary to look at the shape or duration of

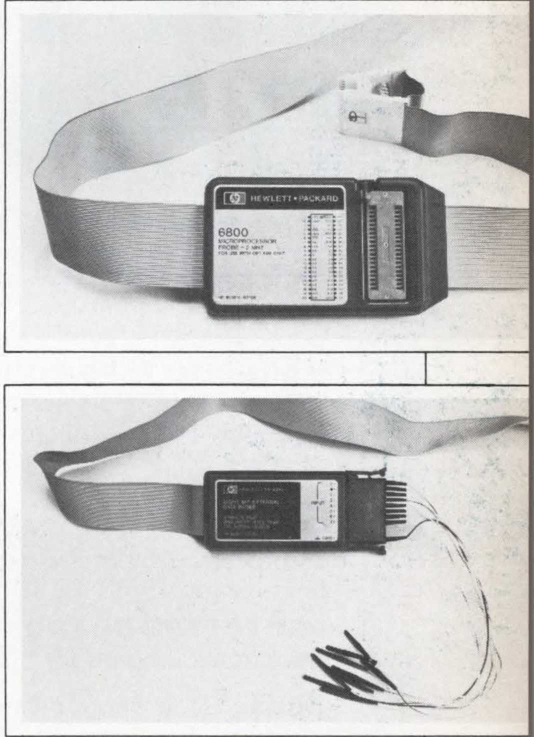

Figure 2: Connection of logic analyzer to μP is via a dedicated module (a) or a general purpose connector (b).

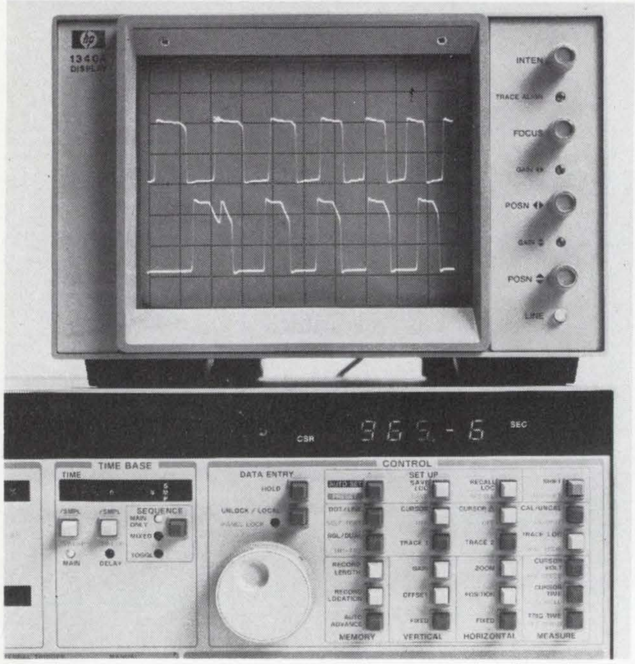

Figure 3: Two signals, recorded in dual channel mode, show why a trigger signal is erratic. Noise, which is high during a particular portion of the μP program, is responsible.

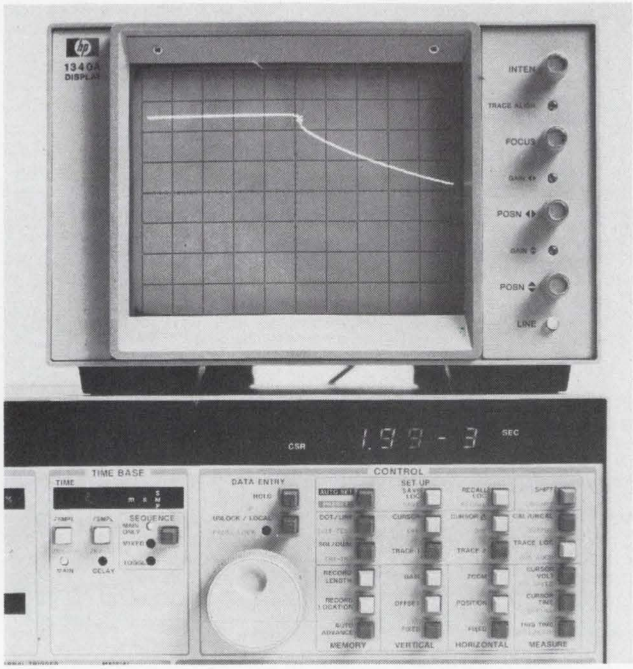

Figure 4: The photo shows the time margin between the end of the power down subroutine (indicated by the intensified trigger point) and the power drop off.

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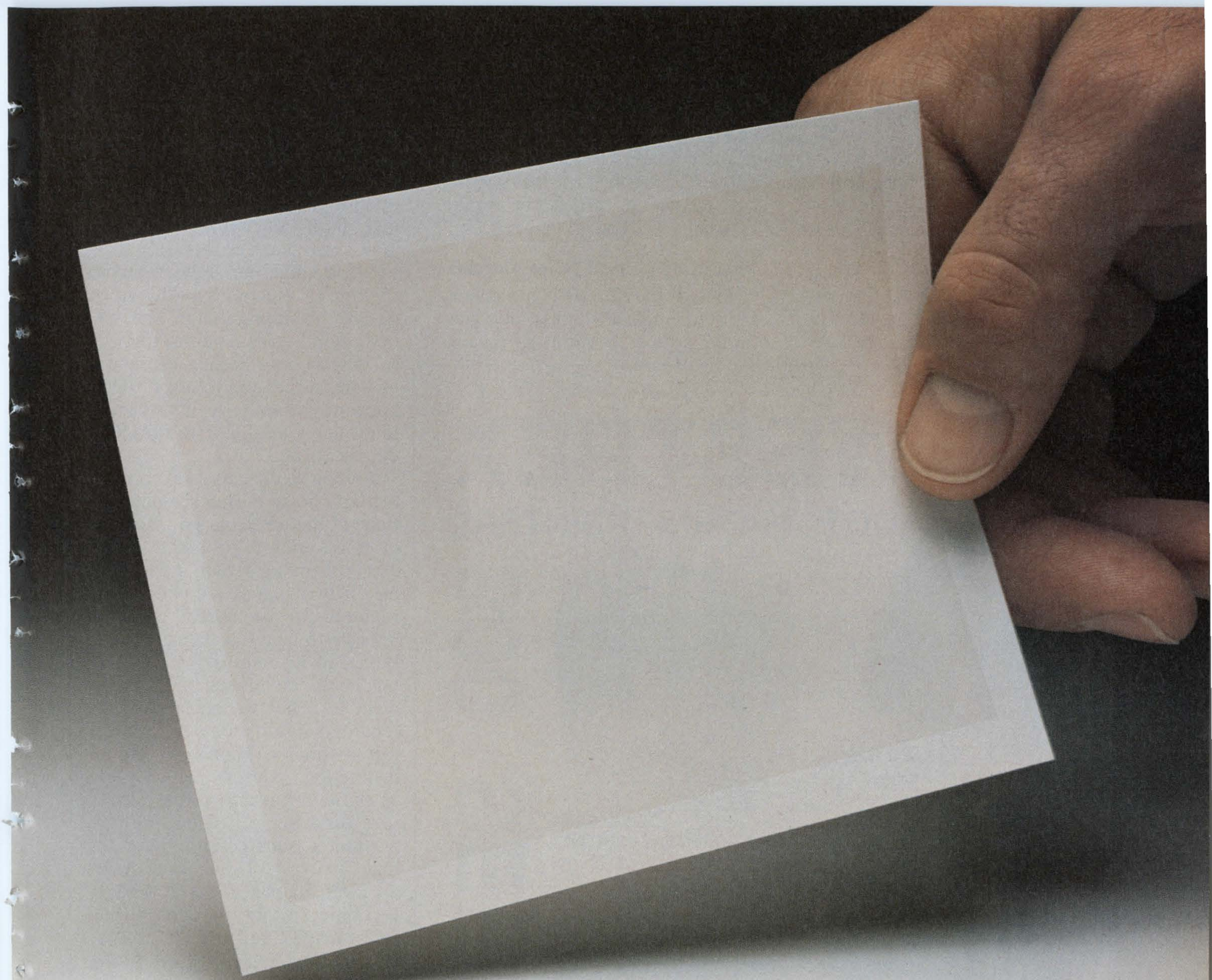

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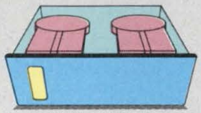

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analog signals, or other changes in waveforms which may not be apparent using a logic analyzer alone. By using a logic analyzer to trigger a waveform recorder at the right time, recording these previously difficult-to-capture signals is easy, and the results obtained are better than have been available before. These two examples of applications show typical signals this procedure would be used to record.

Measuring Critical Noise Margins

In a μP-based system, it is important to measure noise margins during critical portions of the μP program.

For example, during the I/O operation, noise levels are often high; in digital circuitry, this noise may even cause an occasional bit to read high or low when it shouldn't. Recording the noisy signal, beginning when the I/O operation begins, enables the user to determine whether erroneous bits are in fact due to noise. Also, knowing the noise level at critical times helps to eliminate problems due to noise.

Analog signals may also be particularly noisy during specific portions of the μP program, resulting in noise-related problems which are difficult to detect. For example, if two signals (A and B) are required to be "high" simultaneously to generate a trigger, and both signals are noisy, trigger timing could be erratic and unpredictable. The two signals can be recorded simultaneously to check this possibility **(Figure 3).** The μP instruction address which indicates the beginning of the subroutine servicing a trigger may be used as a trace condition for the logic analyzer. This also provides a trigger for the 5180A at the correct time, so that the signals of interest may be recorded.

Record Characteristics Of Power Supply Turnoff

During design or service of a μP-based system, it is often important to look at power supply turnoff characteristics. Most μP-controlled systems have an interrupt which causes the program to go immediately to a power-down subroutine when the μP discovers that power is failing; an instruction address in this subroutine may be used as a trigger condition for the logic analyzer.

For example, if the waveform recorder is triggered when the logic analyzer receives the instruction address indicating the end of the power-down subroutine, it is possible to measure the time margin between the end of the power-down subroutine and the point at which the power supply voltage level is too low to use **(Figure 4).**

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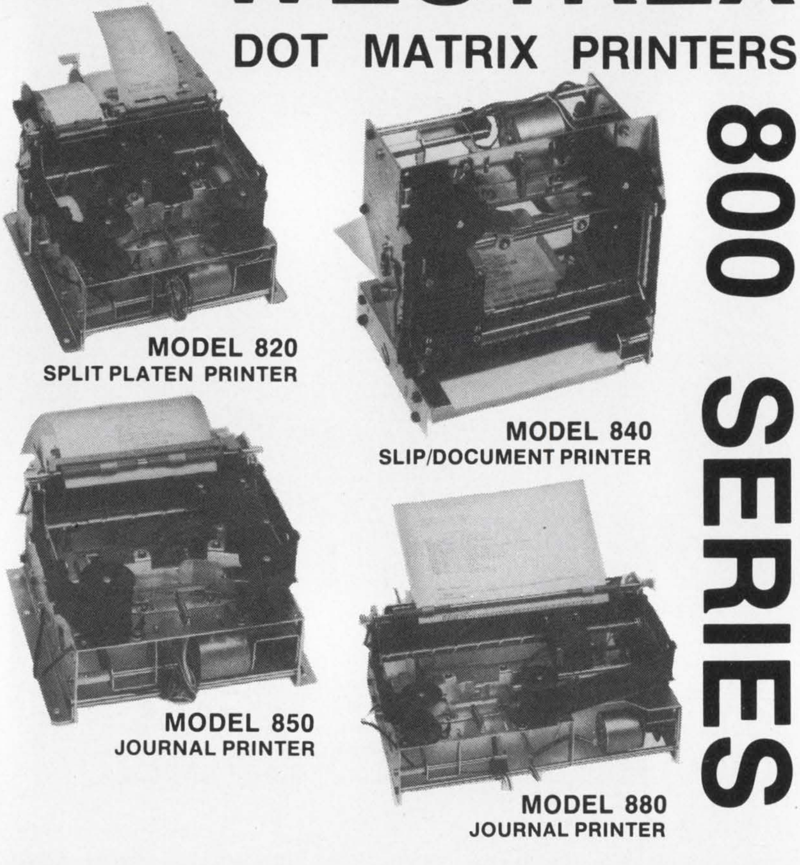

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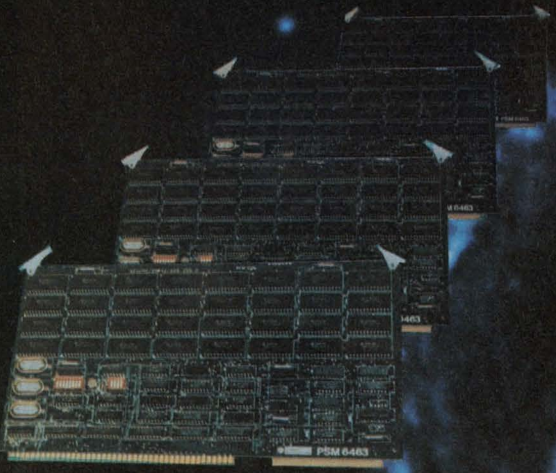

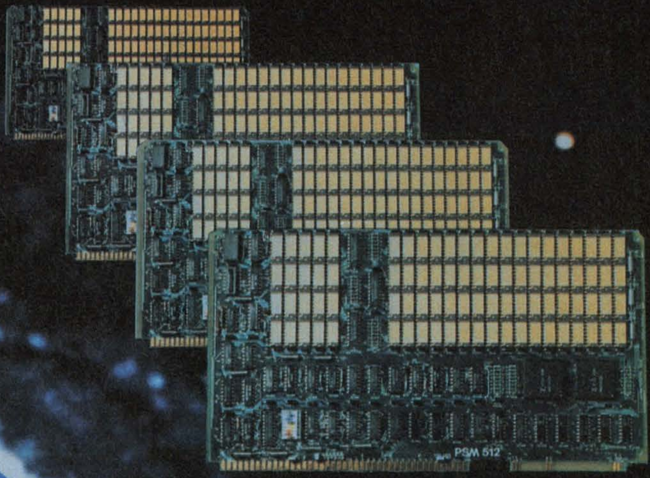

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Next Generation E^2PROMs Ease Design-In Task

Staff Report

E^2PROMs can be electrically programmed in-situ by the OEM or end-user without the inconvenience, time or expense it takes to remove an EPROM from equipment, send it to the service facility, erase and reprogram it and then reinstall it in the field. Until now, designers using these devices in their µC products have had to provide a write and erase voltage as large as 21V, rising through an exponential waveform.

Now, both Seeq Technology Inc (San Jose, CA) and Xicor Inc (Milpitas, CA) plan to introduce 2K × 8 E^2PROMs which need only 5V for writing and erasing and which require no peripheral circuitry to generate RC waveforms. The introduction of these parts will allow self-adaptive computer systems to be made more easily with fewer peripheral circuits. Other E^2PROM manufacturers, such as Motorola, National Semiconductor and Intel, must see this as a great threat to their E^2PROM market, although last year Intel was saying that in the long term the 21V programming voltage would become a standard level for program voltages. To fully appreciate how the new E^2PROMs from Seeq and Xicor will ease the designer's task, an 'industry standard' part—Intel's 2816 2K × 8 E^2PROM will be discussed.

> *Electrically erasable PROMs present today's µC designer with the ultimate in program-store flexibility.*

New Breed of Memory

In 1980, Intel Corp introduced its first E^2PROM, the 2816. The company saw this as the first of a new breed of memory that would eventually become the standard storage medium for µPs, offering a high degree of RAM-like flexibility while retaining the non-volatile characteristics of ROM. To obtain optimal system efficiency, the E^2PROM should respond rapidly to allow the highest possible CPU performance. The 2816 satisfied this requirement with a low access time of 250ns so that program execution was possible directly out of electrically erasable memory. Because the 2816 does not operate solely from a 5V supply, several peripheral circuits are needed in the chip erase mode and for writing and erasing. Should the user wish to erase the entire 2816 array at once, the 2816 chip erase function will only operate when the output enable $(\overline{\text{OE}})$ pin is raised above 9V. When $(\overline{\text{OE}})$ is greater than 9V and the chip enable $(\overline{\text{CE}})$ and Vpp are in the normal write mode, the entire array is erased. This function takes approximately 10ms. The data input pins to the device must be held to a TTL high level during this time. **Figure 1** shows the peripheral circuitry needed to implement an $(\overline{\text{OE}})$ chip erase control.

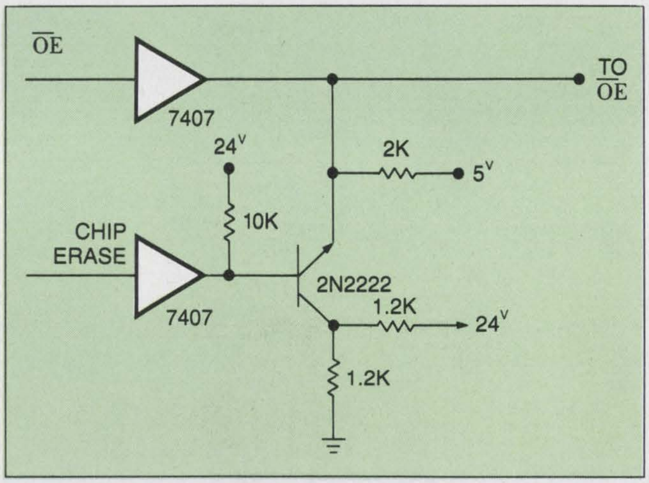
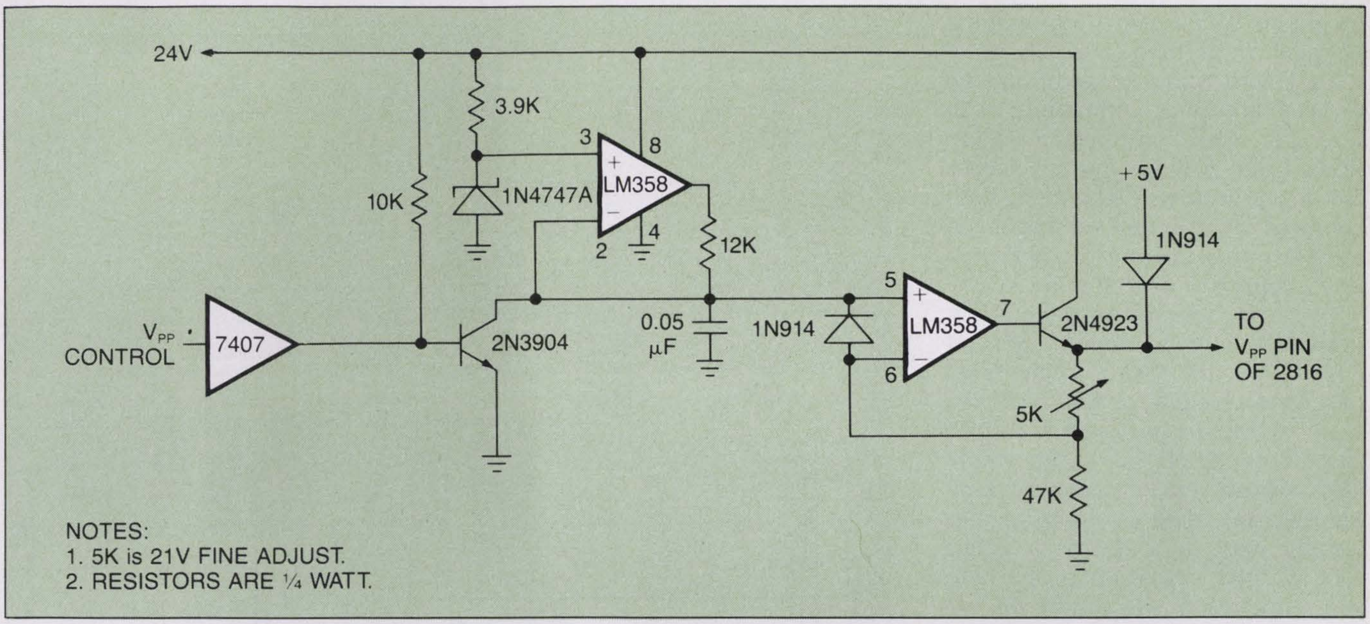


Figure 1: An $\overline{\text{OE}}$ chip erase control must be used with conventional E^2PROMs of the 2816 type.

Another problem facing designers using the 2816 was the shape and value of the Vpp pulse used to ensure long-term reliability and operating characteristics. When using the 2816, the Vpp must rise through an exponential RC waveform. **Figure 2** shows a recommended Vpp switch design, useful where programming will occur over the specified temperature and operating voltage condition. This additional circuitry provides the exponential programming voltage necessary to operate the 2816. Furthermore, to operate this circuit, another circuit may be necessary to provide the 24V needed to operate this switch! In a system environment where this voltage is not available, a switching regulator can be used to convert 5V to 24V (**Figure 3**).



NOTES:
1. 5K is 21V FINE ADJUST.
2. RESISTORS ARE ¼ WATT.

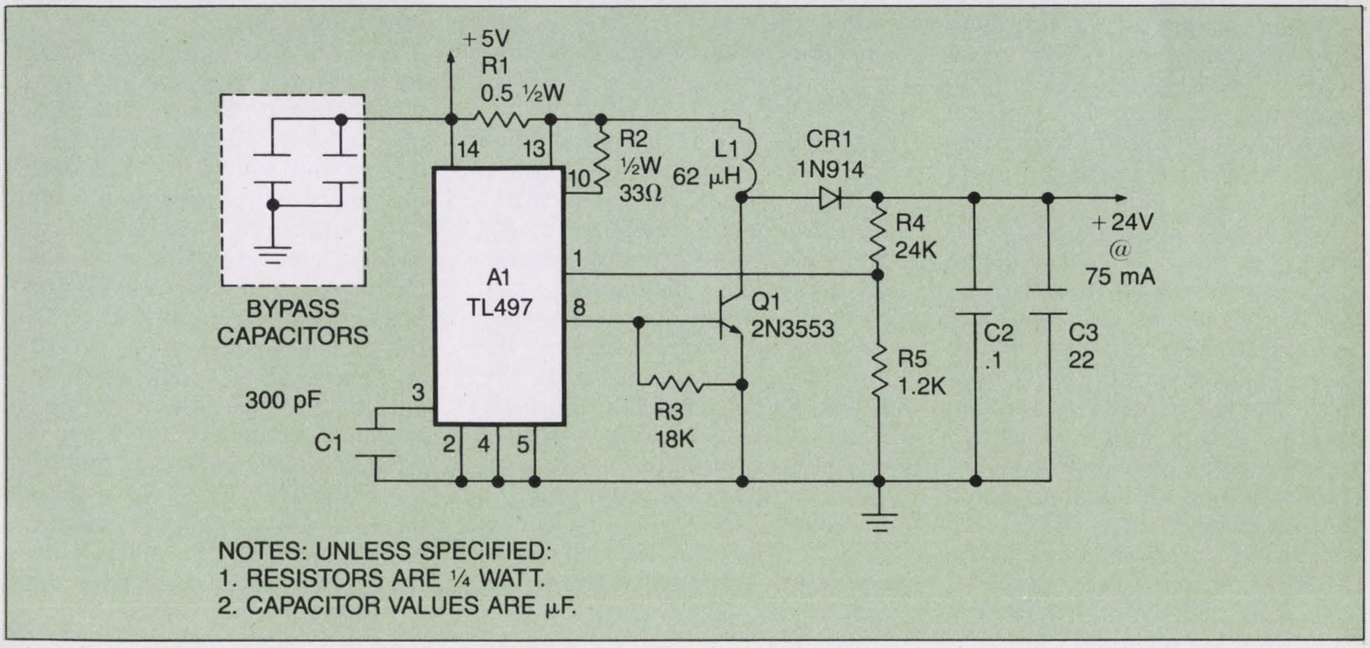
Figure 2: An operational amplifier switch design for Vpp programming of the 2816.

With all the peripheral circuitry needed to implement the E^2PROMs onto a µC board, it seemed only a matter of time before all this peripheral circuitry was implemented on-chip. However, Intel Corp, following the design philosophy that the 21V programming voltage was here to stay, decided to implement everything *but* the 21V programming voltage circuitry on-chip. The result was the 2817 2K × 8 E^2PROM introduced in February. Integrated onto the 2817 is a 16K-bit E^2PROM identical to that of the 2816 plus all the logic and timing circuitry needed to support in-circuit alterability of stored data.

Bob Derby, marketing director of Intel's nonvolatile memory division, has said that with most of this interface logic integrated on-chip, the 2817 simplifies design, reduces total board-space requirements and helps the OEM get his product to market faster.

Devices Aid OEM Design

Helping the OEM ready his product faster—and gaining a substantial part of the E^2PROM market—must have been a concern also at Xicor and Seeq Technology. Both companies have managed to integrate all the peripheral circuitry,



NOTES: UNLESS SPECIFIED:
1. RESISTORS ARE ¼ WATT.
2. CAPACITOR VALUES ARE µF.

Figure 3: Step-up voltage regulator converts 5V to 24V.

including an on-chip programming voltage, onto their 16K 2K × 8 E^{2}PROM devices. In addition, the devices are plug compatible with the 2816 which requires an additional high voltage power supply for programming. Although both companies have not yet produced samples, these should be ready in the second half of this year.

It is also believed that the Xicor part will have an access time of 300ns and the Seeq Technology part an access time as fast as 200ns. Data in Xicor's part, the X2816A, can be modified by using simple TTL signals and a single 5V supply. Storing data is analagous to writing data in a RAM; a 200ns TTL $\overline{\text{STORE}}$ signal initiates a byte store operation which will be executed in a maximum time of 10ms. Since addresses and data are latched, the X2816A frees the system for other tasks during the 10ms period. In addition to the byte modification capability, a 10ms total chip erasure is provided.

Other companies heavily involved in the E^{2}PROM area are National Semiconductor and Motorola. At this year's International Solid State Circuits Conference (**Digital Design,** March 1982, pp. 74) both companies described E^{2}PROMs which follow Intel's philosophy of an external 21V programming voltage, although both integrate on-chip all the necessary logic and timing requirements. National's 16K E^{2}PROM features an access time of 200ns. The part can be written and erased within 10ms by applying a DC signal of 21V to Vpp.

Motorola's 32K E^{2}PROM is organized as 4K × 8 and features a typical access time of 90ns. The device is not only word (1 byte) and array (4096 bytes) erasable but also page (32 bytes or 128 bytes) erasable. The page mode feature allows the system with a structured memory hierarchy to reduce reprogramming time for updating stored data. Assembled in a 28-pin DIP with JEDEC proposed pinouts, the E^{2}PROM is fully static and TTL compatible and requires a 5V supply for READ operation. For programming and erase operations a 21V supply must be used. Whichever vendor is chosen, one thing is certain—with more and more functionality being integrated on-chip, the semiconductor cost/volume learning curve will reduce E^{2}PROM prices to parity with UV E^{2}PROMs by the mid 1980s. In the interim, E^{2}PROMs will be designed into those applications where their cost is offset by the functional value of their flexibility.

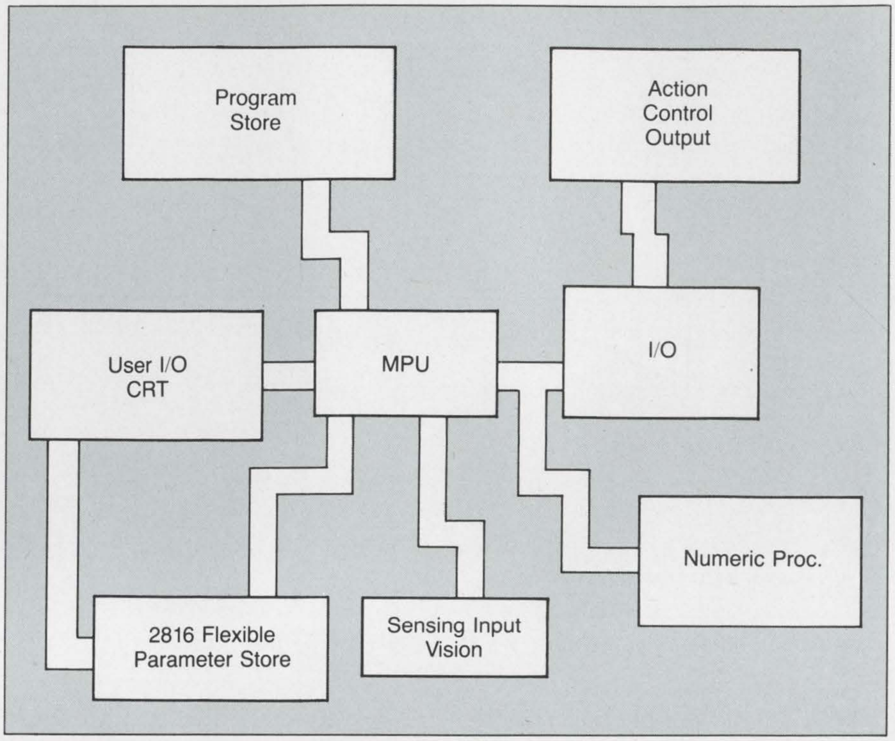


Figure 4: Block diagram of a robotics controller.

Improved Process Control

One market segment that will find E^{2}PROMs attractive is industrial process control. In large plants with distributed processing stations under control of a central computer, E^{2}PROMs can improve local process control and monitoring. Such configurations require the central computer to alter the E^{2}PROM's contents remotely when a change in progress occurs, to optimize local processor operation to the new conditions. The E^{2}PROMs can also be used as data store devices to monitor flow rates and valve closures, thus freeing the central computer for more important duties. Indeed, using E^{2}PROM technology, robotics can be made more efficient through the use of easily reprogrammable motion and action paths. When, say, retooling of a part is necessary, changes can be made simply, easily and cheaply by simply reprogramming the E^{2}PROM memory. No physical system tampering is needed; changes in robot action can be made through a cable or through a remote data link.

In robotics systems, typically the robot's path is contained in a nonvolatile memory device. The μP sequences through the action co-ordinates and directs the path of the machinery. This action path is typically changed infrequently—changes are only made for retooling or for correction of program bugs. However, because these robots are becoming more versatile and are being used for many different applications, the need for a flexible program memory is becoming more important—thus the need for E^{2}PROMs. The system design for such a controller is similar to existing designs. The main distinction is the added capability with E^{2}PROM memory (**Figure 4**).

In this system, where E^{2}PROM is used as an infrequently changed

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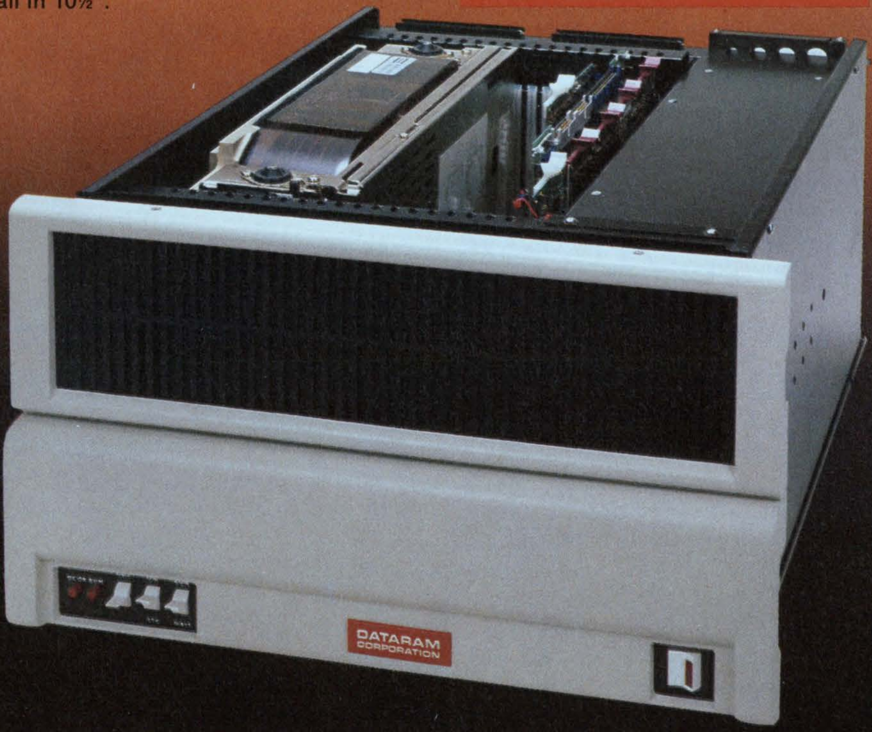

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parameter storage media, changes to E^{2}PROM memory can be made on-line (i.e. the CPU can directly interface to the E^{2}PROM). No arbitration logic would be needed, as the robotics would be in a tooling mode and the CPU could be dedicated to servicing the E^{2}PROM. The system's memory map would be partitioned in such a way so as to locate E^{2}PROM memory in the flexible portion of memory space. This flexible memory could contain set points, motion or control paths that need to be non-volatile but still can be changed dynamically while in the system. The E^{2}PROM can also contain program routines that would undergo change by the end user. This essentially allows the user to custom fit the system to require service from an equipment vendor. Such an approach reduces service costs and extends the useful life of the machine by minimizing obsolescence.

Point-of-Sale Applications

Another application for E^{2}PROMs is in point-of-sale terminals where they function as look-up tables whose contents—product pricing for example—do not change frequently. The central computer can poll and update the E^{2}PROMs after business hours to monitor sales volumes and adjust pricing to inflation. These needs have been satisfied in the past with E^{2}PROMs which, while low cost, dense and non-volatile, cannot be changed in the field without the use of a service technician. CMOS and battery back-up offer more flexibility at lower density, but can suffer reliability problems. E^{2}PROMs, however, offer EPROM characteristics with the advantages of battery backed-up RAM.

Look-up tables can be stored in a non-volatile way but can be altered in-situ. **Figure 5** shows the block diagram for such a system. The terminal is composed of a high performance μC. In addition, 2816-type memories are used as data and look-up table storage. The typical I/O device structure for a terminal also exists in the system as shown. The serial I/O link provides the system with a remote configuration capability; the contents of the E^{2}PROM can be changed from a central location without the need for servicing.

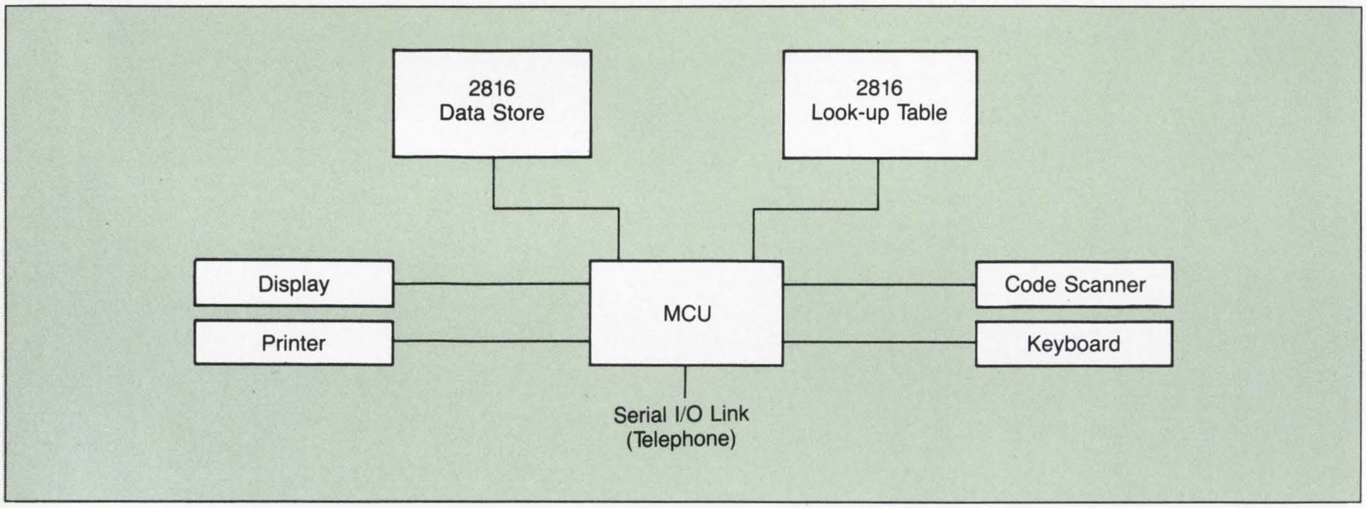

Figure 5: Block diagram of a point-of-sale terminal.

The look-up table contains product description and pricing information. Once the table has been written, the CPU can read from it as necessary to translate product entry codes to price information. If for some reason the table data needs to be changed for pricing or product updates, then the central computer simply sends update commands and new data to the remote point-of-sale processor. Since all remote terminals are linked together at a central location and are in periodic communication with each other, such an update can occur as part of normal inter-processor communication.

In summary, flexibility and greatly reduced service costs will be the key to new E^{2}PROM designs. Easier configurability will also become a key factor in the use of the memories when the Xicor and Seeq parts become available. All eyes must now focus on Intel, National and Motorola—will they or won't they introduce 5V only parts? □

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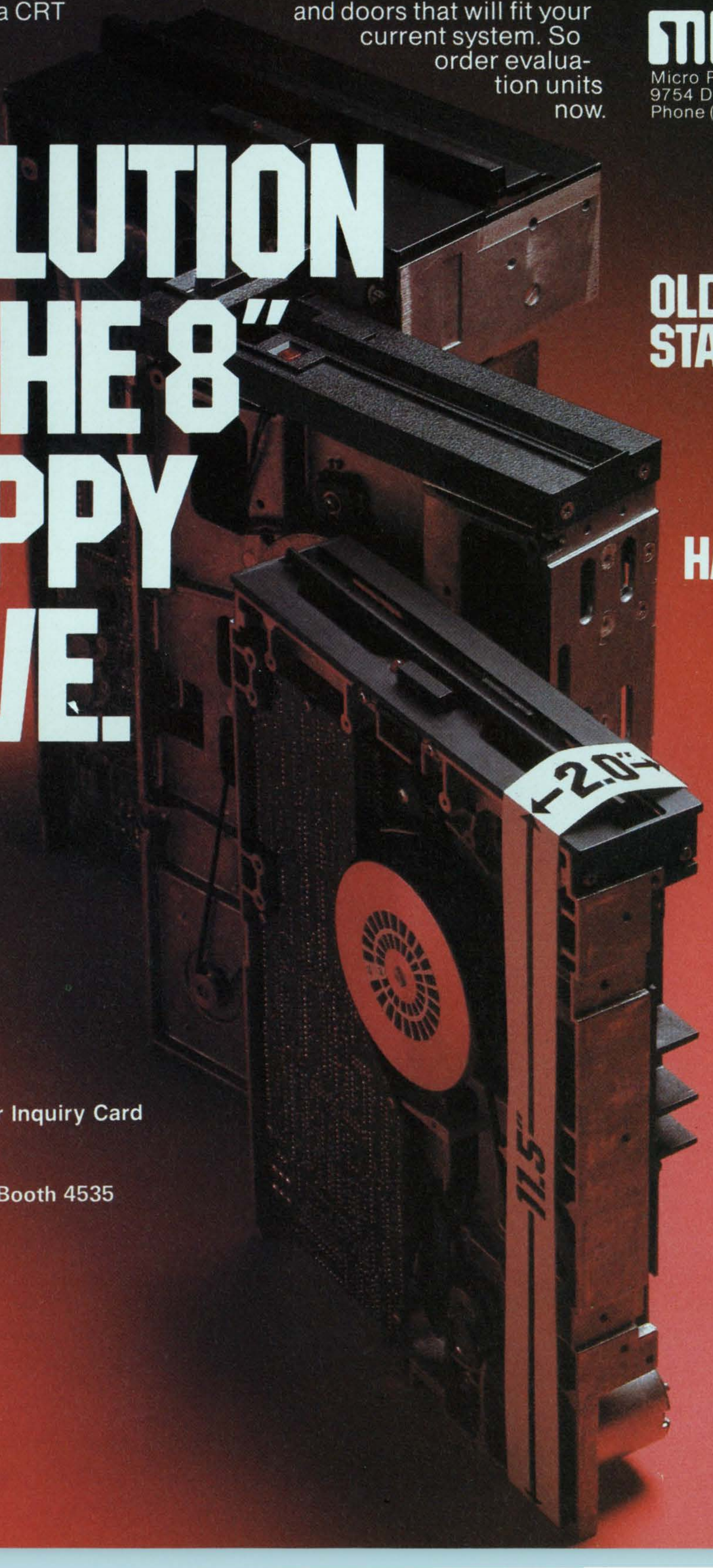

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Computing Power Boosts Speech Quality

Staff Report

At this year's International Solid State Circuits Conference (*Digital Design,* March, 1982), the application of ICs to speech synthesis and recognition had become sufficiently important to demand a complete session. According to Robert Brodersen, who chaired the session, this is indicative of the fact that speech IC technology is on the threshold of an expansion, with an estimated market of $1.3 billion by the end of the decade. For this level of sales to be reached, many new applications for speech I/O will have to be identified. This article looks at both speech synthesis and voice recognition, some of the products now available, and how these products may be used to increase the man/machine efficiency of computer systems.

Speech Gains Practicality

Up to now, speech synthesis systems have either been very high quality, extremely expensive systems or mechanical-sounding and relatively inexpensive. In the past few years, however, quality speech synthesis has become economically feasible as a result of data compression schemes that have been developed to produce intelligible speech employing LSI circuits.

The goal of any speech synthesis technique is to reduce the number of bits that must be stored to reproduce the human voice. The three technologies currently in favor include waveform analysis, phoneme coding and linear predictive coding (LPC). In waveform analysis the machine analyzes the analog waveform produced by the human voice, digitizes it and converts it back at a later date to an analog waveform. Due to the high bit rate involved, this method can produce very high quality speech. However, the large amount of storage required in such systems means that they can be more expensive than single-chip solutions. One advantage is that they are capable of storing a large data base of spoken words.

Mimic Electronics (Acton, MA) has produced such a speech processing unit. The system converts an audio signal into a digital bit stream which can be sampled by a computer, stored and played back through the system. A data rate of 9600 bits per second (bps) produces high speech quality and is capable of storing a 400 word vocabulary on an 8″ floppy disk. Similarly, the sixteen hexadecimal digits "0" to "F" can be spoken from the data stored in 8K bytes of RAM or ROM.

According to Mimic, the speech storage memory need not be high quality, and slow memory chips or chips with a few random bit failures can be used. This is because each bit in the serial data output

stream is independent of any other bit. Designed primarily for consumer products such as toys and video games, the Mimic speech synthesizer requires no A/D or D/A converters and interfaces to computers and communication systems.

With parametric waveform recording (PWC) digital code generated from voice input is converted back to analog; then the synthesized waveform is compared to the original.

Phonemes Ease Memory Demand

In phoneme coding, the speech system stores phonemes, the basic phonetic sounds of human speech (there are about 65 in English) and puts them together to form words. The advantage of this method of speech synthesis is the very small amount of memory capacity required by the system. Votrax, a division of Federal Screw Works (Troy, MI) is currently offering a pair of board level products based on this method of synthesis.

The company's speech access phoneme controller is a circuit board that contains an SC-01 speech synthesizer, a stored vocabulary of up to 511 words and on-board amplifier. A more versatile unit, the Speech module 1, provides 1300 words in its expandable vocabulary and is capable of speech in English, French, German, Italian and Spanish. The unit is available in either board-level, stand alone or rack-mounted configurations.

LPC speech systems use a mathematical model of the human vocal cords to generate parameters in digital code of human speech. The digital coding is then converted into an analog waveform to produce spoken words. LPC requires low bit rates and has gained public awareness through its use by Texas Instruments in its Speak and Spell toys.

In November last year, Telesensory Speech Systems of Palo Alto introduced its Speech 1000 board, a synthesizer capable of receiving encoded speech data from an external mass storage device such as a floppy or hard disk **(Figure 1)**. The board uses downloadable RAMs instead of programmed ROMs to temporarily store one of many 64 kbit data files stored externally. Each file contains approximately 30 secs of speech compressed and encoded using LPC. This, the company claims, allows OEMs, systems integrators and end users to change or expand the system's vocabulary without hardware modifications.

In operation, a command from the host computer will instruct the Speech 1000 board to receive a vocabulary data file and store it in RAM. When the download operation is completed, another command instructs the board to enter the synthesis mode. In this mode, other commands are sent by the host to tell it what to say. By arranging the commands and word pointers in a desired sequence, the synthesizer board will execute the sequence of commands to speak the arrangements of words or phrases.

Of the techniques available in speech synthesis, phoneme synthesis can produce speech from low data rates and is often used in systems where memory is at a premium. Waveform analysis and LPC techniques are popular when a mass storage device is available. Many systems in the future will require an almost unlimited vocabulary that is clearly spoken.

Alan Yatagai, Telesensory's marketing manager for the Speech 1000 board, claims that typical synthesizer systems having the vocabulary stored in ROM limits the hardware to a specific application and also complicates any upgrade of the system's performance. Another company that would seem to agree with this theory is Centigram Corp. (Sunnyvale, CA). At Centigram, a technology has been developed which combines the best of linear predictive coding (low bit rates) with that of waveform analysis (high data storage).

Called parametric waveform coding (PWC), the new technology has been used to design a voice output terminal called LISA and a development system that performs the speech analysis for LISA **(Figure 2)**. The development system can create real-time voice for virtually any application, the company claims. Because the digitized voice is stored on disk, the storage capacity of the system is unlimited.

When spoken voice is input into the system, digital code is generated. The digital code is converted back to an analog waveform, and waveform analysis is used to com-

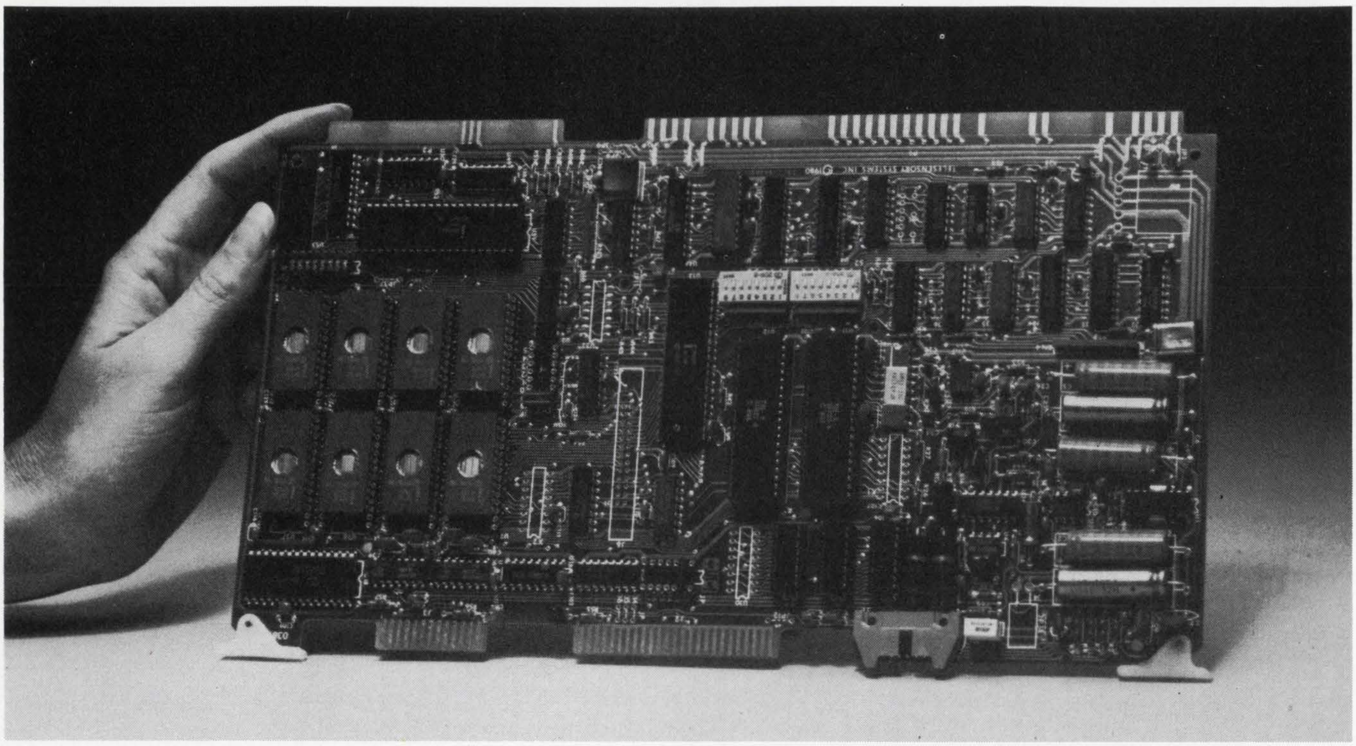

Figure 1: Telesensory's Speech 1000 synthesizer board is controlled by a host computer through the use of commands and pointers.

pare the synthesized waveform with the original. If the synthesized voice is not accurate, the system continues to compare and correct until the waveforms match. The system then plays the digitized version back to the user who can edit it with other phrases before storing it on disk. The digitized voice looks like standard text characters to the computer, allowing the computer to manipulate the bit stream without the use of additional software. By digitizing voice in real time, the user avoids the costs and turnaround time of factory-generated speech.

Voice Recognition Systems

Voice recognition systems may be divided into two categories—speaker dependent and speaker independent. In both systems, the input word to be identified is converted into electrical signals by a microphone and then processed to extract a set of identifying characteristics called descriptors.

In existing systems, these descriptors may be zero crossover detectors, average energies in certain bands of frequencies, formant frequencies and bandwidths and/or PARCOR co-efficients. These descriptors are compared to a prestored library of reference descriptors, or templates, to obtain a best fit. A system that uses a set of reference templates from a large population is called "speaker independent" whereas a system that uses a set of templates created by a single speaker is called "speaker dependent." The speech templates are loaded from the user's I/O device into the unit's memory.

Word-inputting is performed in a soundproof room, so that background noises will not affect the templates. If the units are to be used in an industrial environment, such as on a loading dock, on a production line or noisy surrounding, noise-cancellation microphones can be used. Generally, such units can cancel out or compensate for steady-state noise, such as the hum of an AC motor.

In speech recognition techniques, tradeoffs exist, and lower cost systems generally have smaller vocabulary sizes, lower recognition accuracies and discrete-word, rather than continuous-speech, recognition capability. Two products on the market today that do have the capability to recognize limited forms of connected speech are available from NEC **(Figure 3)** and Verbex.

Digital Filtering

In a typical speech recognition application using digital filtering, the voice input signal is sampled at discrete time intervals. Each sample is A/D converted into a digital word. Then, the digital filter operates on this digital input sequence to form an output sequence that is fed into a DAC that converts it into a pulse train, with each pulse area equal to the inter-sampling time multiplied by the respective sequence value.

Recovering the continuous output is easy: an analog RC lowpass filter simply smooths it out. In addition to the earlier-mentioned advantages, the two sampled data signal outputs (from the ADC and the CPU filter) are easily analyzed in Z-transforms and implemented more easily.

Unfortunately, digital filters can prove expensive; a 16-channel filter can add up to $200 to a word rec-

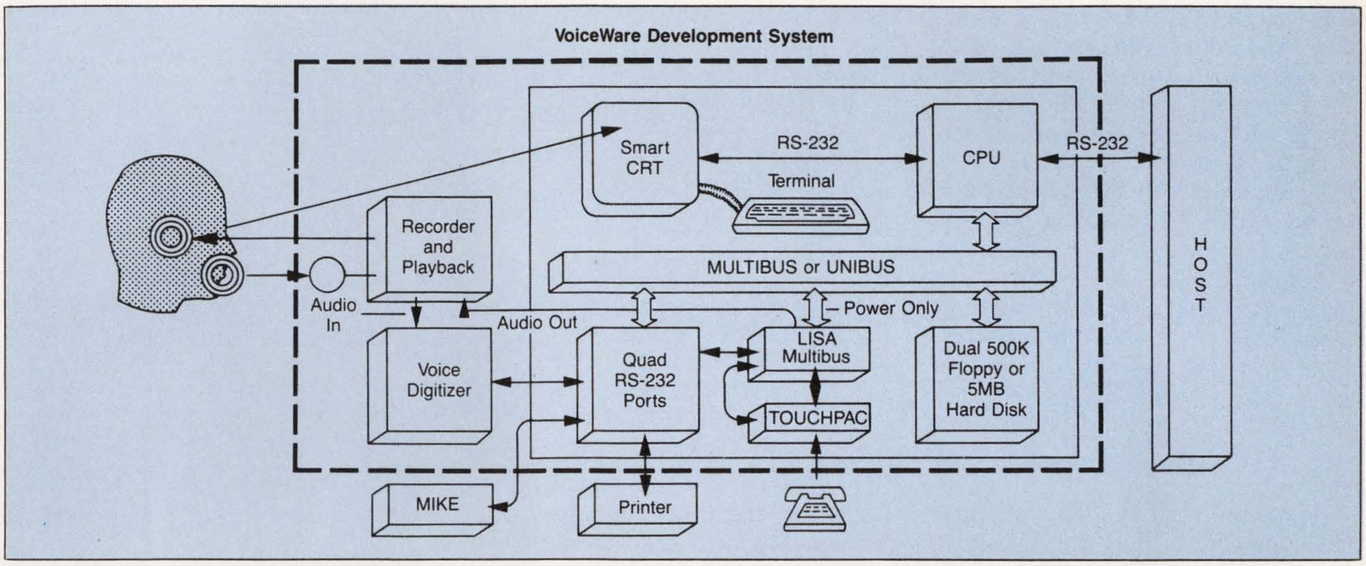

Figure 2: Centigram's Voiceware Development System provides unlimited speech capabilities for almost any computer system.

ognition unit. It is possible to have 16 logarithmically-spaced bands, yet use only one analog filter by using a digital shift register buffer (spinner). This technique, used in Centigram's "Mike" system, makes the filter do multiple duty by "spinning" the signal, after passing through an ADC, through the filter 16 times. Each time the rate is faster. After passing out of the "spinner," the signal passes through a DAC before being filtered, after which it is reconverted to digital form by a second ADC. In essence, what the spinner buffer is doing is shifting or selecting the desired frequency and aligning it with the analog filter's center frequency. This digital-analog hybrid technique cuts down on filter costs.

Once this spectral data, which is in 16 bands, is digitized by the second ADC, it goes through a word-framing process that detects inter-word demarcations or boundaries and then "stretches" or "compresses" each word to a given, pre-fixed duration. This compensates for different speaking rates. In "Mike," speakers must pause 100 ms or longer between words. When total spectral energy rises above (or falls under) a given threshold, the word is "framed" and considered to be a word.

This framed word consists of 25-ms-wide time increments, each consisting of the logarithmically-spaced frequency bands. Mike reduces this data to a 240-bit string. During "training," Mike ORs this string with the other samples (for each vocabulary word) spoken to it. This produces an average template.

When in the recognition mode, the incoming string is ANDed with the template bits, thus producing a new string which can be operated upon by an algorithm(s) to produce scores. If above a predetermined threshold, and above the next-highest score for the second most likely template, then the unit selects this to be the word. The threshold can often be varied by the user. As expected, a high threshold means low sensitivity, and the rejection rate for false identifications rises. On the other extreme, setting a low threshold guarantees a low rejection rate, but

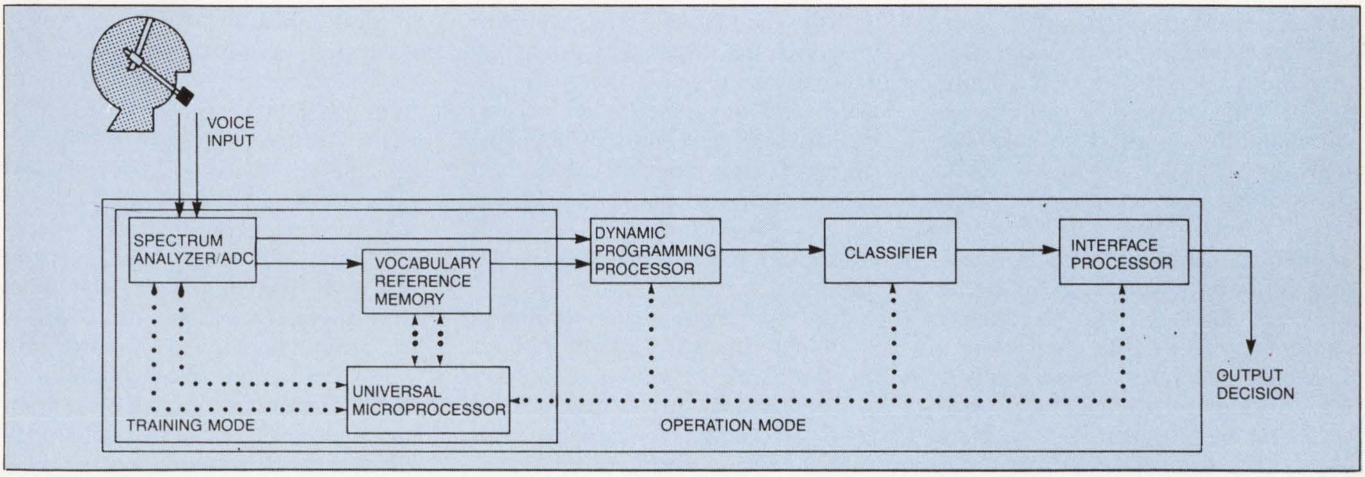

Figure 3: NEC's DP-200 speech recognition system uses a technique they call Dynamic Programming.

also increases the error rate. Whatever the threshold setting, if a framed word cannot meet or exceed the recognition threshold, a signal of "no recognition" is fed back to the user.

Some units will list the top five or so words from the last set of words recognized. This command is helpful in identifying bad training procedure or similar-sounding words. If the associated recognition scores of the top two template words are too close, then the user can retrain the unit by deleting the close word and adding a different one.

Some units go further and provide diagnostics that can also provide feedback, such as the Auricle-1 from Auricle (Cupertino, CA). This unit allows the user to display the 16 filterbank energy values. Each filter output signal is put through a lowpass filter, rectified, and then digitized with a logarithmic ADC. The 16 digitized numbers range from 0 (no energy) to 127 (maximum spectral energy).

Isolating Interword Gaps

One problem in speech recognition is isolating interword gaps. Even a carefully-trained operator can occasionally shorten these gaps, causing words to be falsely recognized as syllables. Conversely, syllables can be mistaken for words, particularly if the operator hesitates due to momentary uncertainty.

A way to avoid the 0.1 to 0.2 sec. interword gap or pause trouble is to subdivide all words. The 180 wpm Threshold Technology "Quiktalk" does exactly this; it divides each word into 16 equal time increments and from each obtains 32 spectral components from a 32-channel filter bank. It breaks the input into a 1024-bit array which is then compared to template patterns. After making an initial estimate of word boundaries, the system refines the guesses. First, the word is analyzed for frequency content and time rate changes in a spectrum analyzer. An acoustic feature detector then detects word ends; when it detects a complete word, it begins time-processing. Secondly, a time normalizer breaks the word into equal time increments, as mentioned above. Inputting into the time normalizer is a dual mode switch, so the user can select either the training mode or the recognition mode, in which a classifier checks the word against templates stored in memory. Then, a 16-bit micro outputs commands. These vary, depending upon the recognized word. These will control whatever I/O devices the OEM has interfaced to the system, be they disk drives, interfaces to other CPUs, printers, VDTs, tape drives or whatever. A display also provides feedback to the operator. An expansion memory module enables a 370-word recognition capability. With 180 wpm speed, over-99% accuracy and continuous speech recognition capability, these units provide a more humanlike interface.

By omitting or interpolating time increments, lower-cost units adjust words of different duration to a standard length. Better units warp the template by dynamic programming to match the templates in a best-fit. Unlike the simple linear interpolation technique, dynamic programming can alter certain word portions more than others, based upon the results of linguistic study. Every speaker does not evenly and linearly shorten or extend spoken words, so the linear interpolation technique loses something in accuracy.

To circumvent this problem, nonlinear timewarping interpolates the template sections until a best-fit is reached. Since this is only done for template segments, and not the whole template uniformly, this is more accurate.

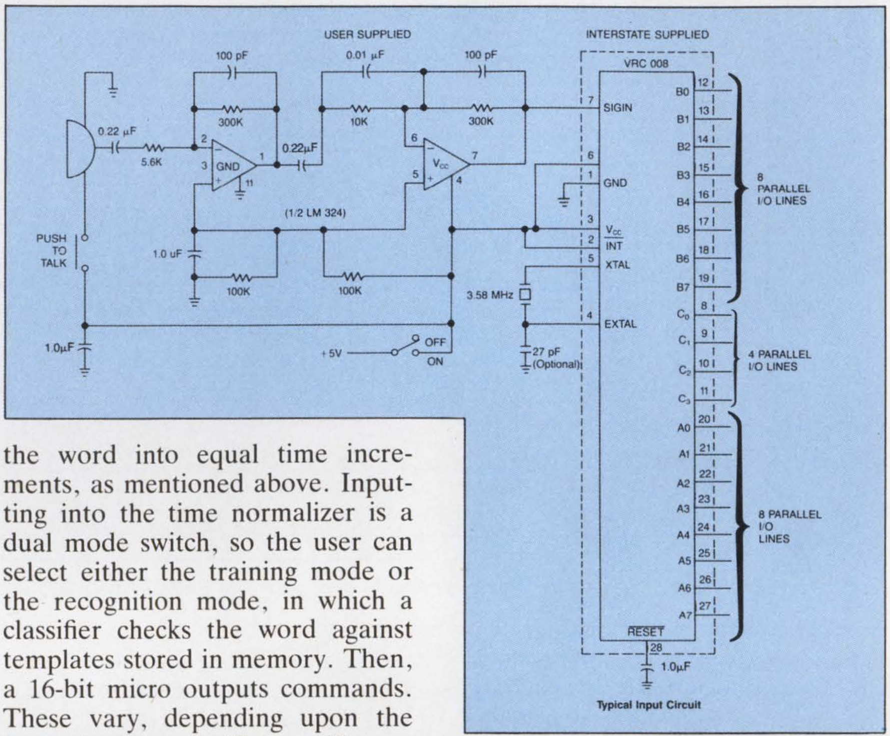

Figure 4: Interstate Electronics Corp's voice recognition chip, the VRC008, is designed for a wide variety of high-volume consumer applications.

Accuracy Vs. Cost

Accuracy of these various techniques is roughly a function of cost. In recent testing, the 16-channel filter technique showed a ZVC error rate of 2.9% to 12.6%. This is what $2.5K will buy. For $70K or so, you can get under 0.15%.

To improve speech recognition reliability, more sophisticated units examine the word in context. Thus, homonyms (words that have different meanings but that are identical in pronounciation) can be readily identified, as can other words. Statistically, certain words are more likely to follow a given word. This is the "branching factor," and can be quantitatively measured. At present no system is available to handle such combinational tree-searching routines, especially in real time. At this stage, the most sophisticated system—used solely for research—is a 1K word, 50-word branching factor system at IBM. Combinational tree-searching takes over one hour to identify 20 seconds of human speech!

Fortunately, many systems sim-

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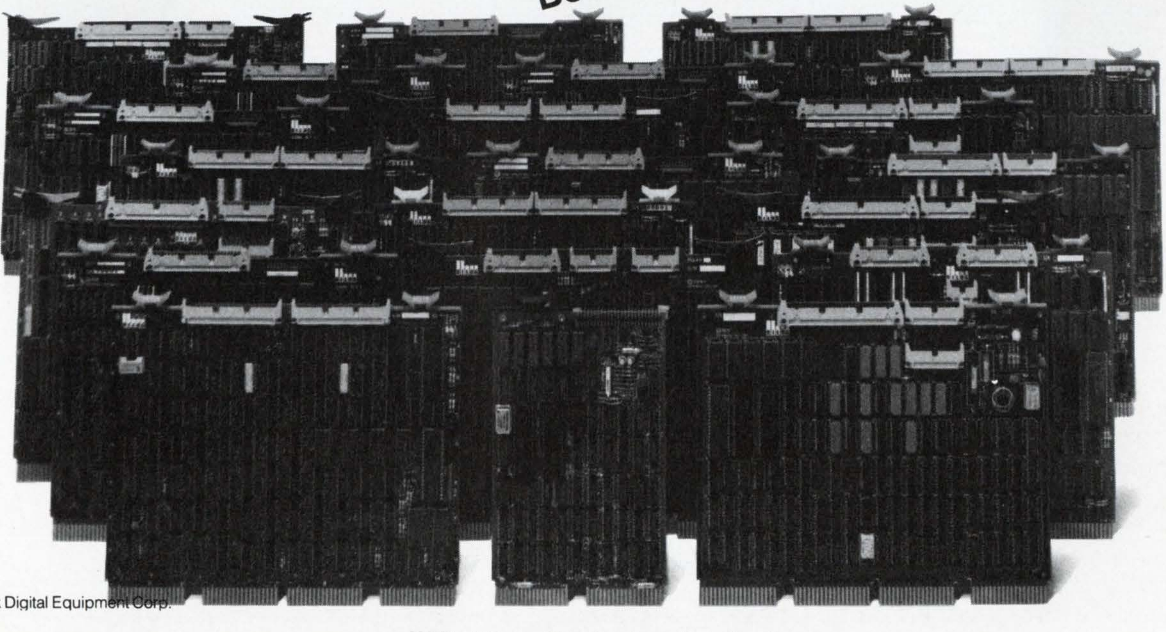

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ply do not need such complicated continuous-speech units, and a specialized, limited vocabulary suffices. Tree-searching state diagram algorithms with limited vocabularies are easily handled by existing micros. Such formal, carefully-defined, finite-state grammars permit existing technology to achieve high recognition without high costs.

To circumvent the combinational explosion for larger-vocabulary systems, another approach is being explored: that of phoneme recognition. Phonemes, the smallest units of speech, number only 40 (16 vowel and 24 consonant sounds), and this lowers template storage requirements considerably. Word recognition using phonemes is very difficult, however, due to coarticulation (sound-modifying) problems. Contextual methods will be used to identify close matches.

Activity on the other opposite side of this technology, the very low end, is picking up. Voice recognition chips and chip sets with limited vocabularies—typically about 16—are now available. Claimed to be speaker independent and 90% accurate for the general population, these chips use a specific vocabulary defined by the OEM, which is then customized for the specific functions the OEM's product will perform. Interstate Electronic Corp's VRC008 is an example of a low-cost single-chip solution **(Figure 4)**. Designed for applications which include toys, games and other voice automation products, the system is speaker independent and can recognize eight spoken words or phrases.

In a typical application "wake up" would activate the system into a receptive mode and prepare it to accept input speech. When the word "relax" is spoken, the system would stop. Programmable for a selected vocabulary, the chip recognizes speech by detecting significant parameters in the incoming word or phrase and comparing them with the stored sequence of a prespecified vocabulary. After the chip has recognized the incoming voice signal, a bit pattern is output for the word number identified.

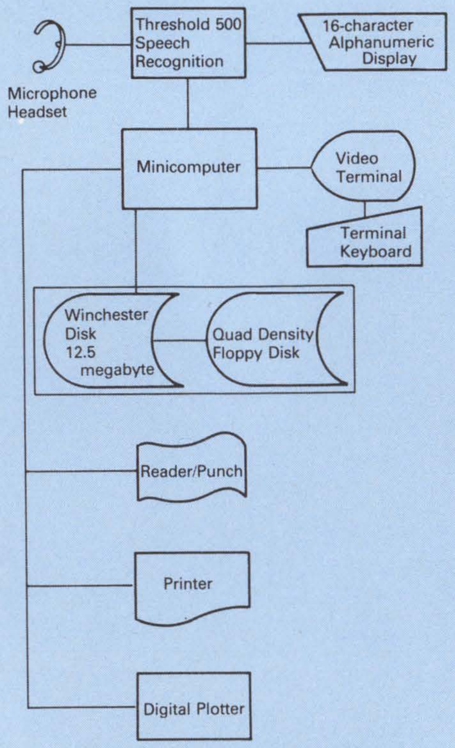
More Computing Power

Speech recognition and synthesis devices have to be chosen on a cost/effectiveness basis as do most other products. However, many manufacturers have now realized that there is no way to produce systems capable of storing and reproducing large vocabularies without resorting to some kind of computing power. Indeed, the computer capable of listening and talking in any language is only held back by the large amount of computing power and memory that this would entail. With the reduction in cost of computer memory systems, it seems likely that such a system will be feasible at least by the end of this decade. □

Maul Brothers—A Faster Way To Bottle

Joe Reitenour of Maul Brothers, the country's largest manufacturer of automatic bottle manufacturing machinery, talks to his computer every day. As Senior Programmer at Maul, Reitenour claims that since he began producing machine tool tapes by voice, per-piece programming time has fallen by 65% to 90%. Maul has eighteen numerical control tools, all of which had to be numerically programmed before the company started using Threshold Technology's Numerical Voice Control System.

"Within a few weeks of start-up we were pumping out error free tool tapes at an unbelievable clip," says Reitenour. "Since parts programming time had been cut, we were able to keep our machine tools busy more of the time and we were tackling programming jobs we wouldn't have thought feasible a few months ago."



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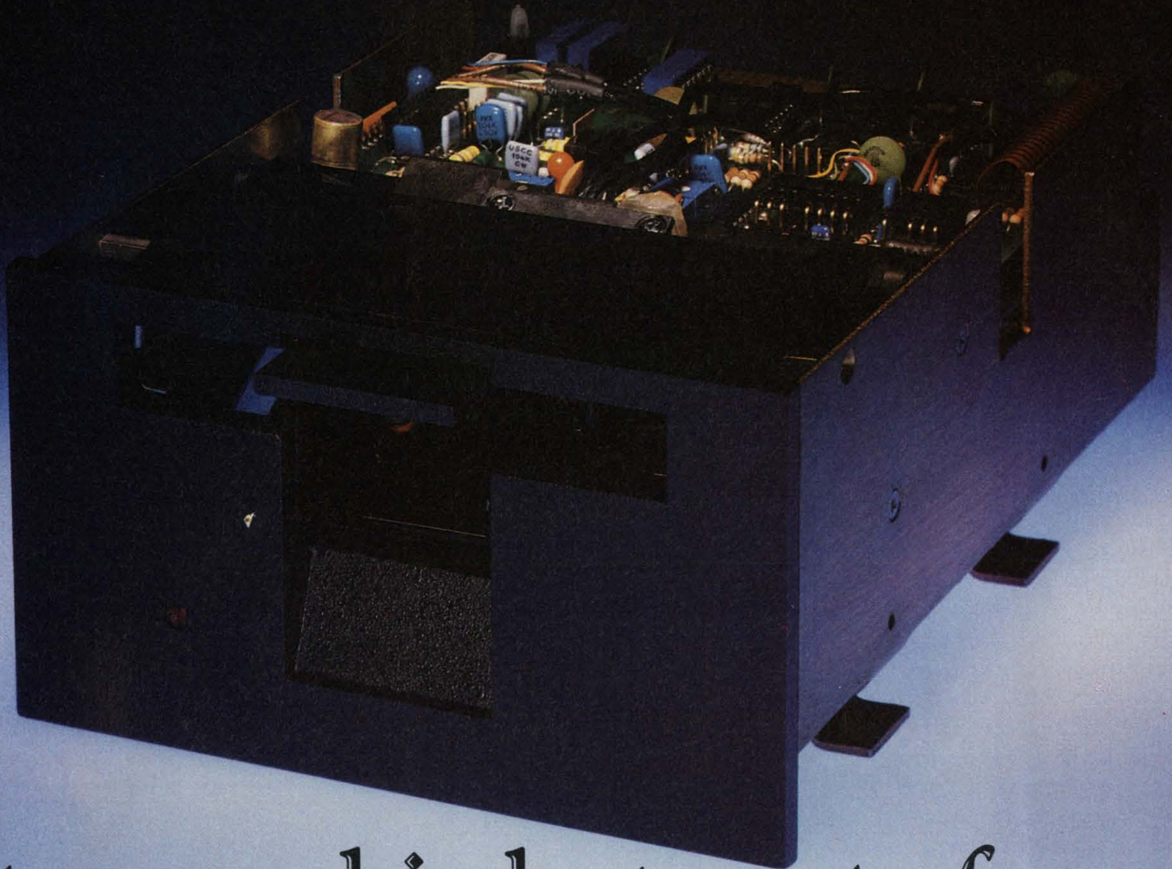

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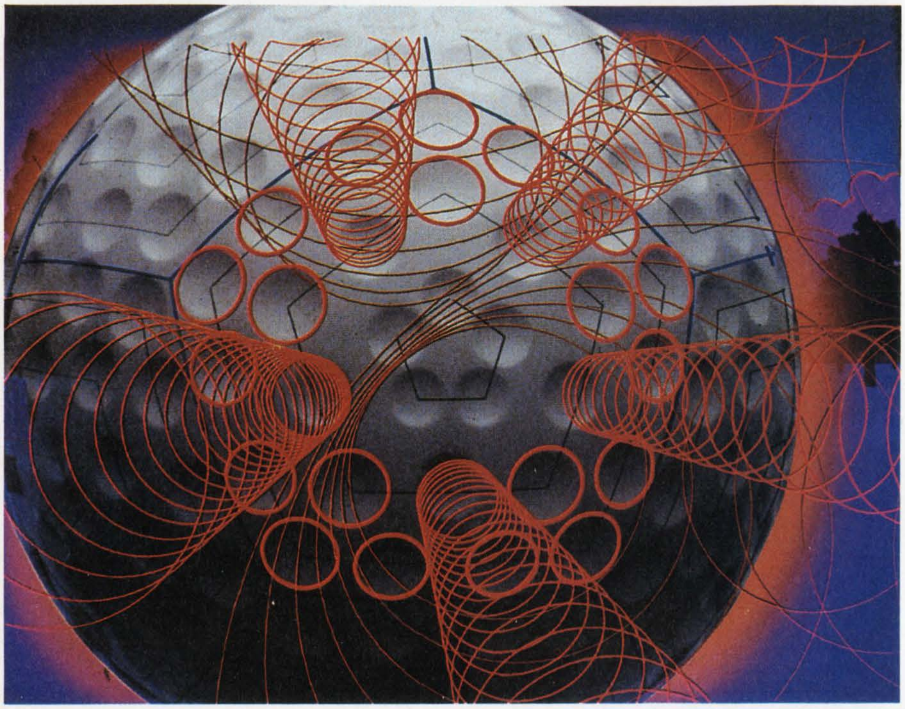

Figure 1: Computer-assisted animation is one of the more exciting applications of computer graphics, as illustrated by this Maxifli 736 "Energy" commercial (courtesy Robert Abel & Associates).

NCGA '82:

Twice the size of last year's NCGA, this year's conference offers a diverse assortment of computer graphics exhibits, tutorials and technical sessions.

by Bob Hirshon

Thirty years ago, a conference on the computer industry could have been held in a hotel suite—today we have NCC. Ten years ago, computer graphics conferences drew small groups of hard-nosed graphics fans. Today, growth of graphics shows rivals the growth of the early computer conferences. And while the NCC growth has leveled off, NCGA (2033 M St, NW, Suite 30, Washington, DC 20036) and SIGGRAPH (111 E. Wacker Dr, Chicago, IL 60601), the two major computer graphics shows, are currently enjoying their highest growth rates ever.

The National Computer Graphics Association will be holding its conference June 13–17 in Anaheim, and expects 20,000 attendees, more than double last year's attendance. Over 120 exhibitors will occupy 125,000 sq. feet of floor space, and 225 speakers at 85 tutorials and technical sessions will address every aspect of computer graphics, from cartography to cartoons.

Sessions and Tutorials

The breadth of the technical sessions illustrates the wide subject area encompassed by the term "computer graphics." NCGA planners were hard-pressed to limit the sessions to the following 17 categories: Animation, Architectural and Engineering CAD, Business and Technical Data Graphics, Defense Automation, Device Independent Graphics, Electrical CAD/CAM, Frontier Applications In Research, Graphic Arts and Media, Graphics for Machine-Mediated Learning, Hardware and Software Standards and Directions for the 80s, Mapping and Cartography, Mechanical CAD/CAM, Medgraph, Petro-chemical Graphics, Statistical Graphics, University Graphics, and Videotechnology.

The CAD/CAM sessions focus far more heavily on CAD than on CAM. VLSI and PC board design dominate the electrical CAD/CAM tutorials and technical sessions. The mechanical CAD/CAM courses focus primarily on setting up a CAD/CAM system, as opposed to using one. A separate group of sessions on Architecture and Engineering CAD explores the possibilities of CAD for solving architecture/engineering problems.

A one-day animation tutorial features lecturers from Digital Video Systems, Lucasfilm, Jet Propulsion Lab, Hanna-Barbera, Digital Effects and others. Topics will include hardware and software, animation techniques, and image processing as an animation tool.

Three days of Defense Automation sessions will cover applications that combine computer graphics and the military. This includes everything from using CAD/CAM for Naval shipbuilding to using computer graphics to help speed up your next military proposal.

Single-day sessions will explore Device Independent Graphics and the concept of a "virtual" graphics device; Graphic Arts and Media, including the role of the artist in the new computer/artist partnership now evolving in the graphic arts; Graphics for Machine-Mediated Learning, which discusses com-

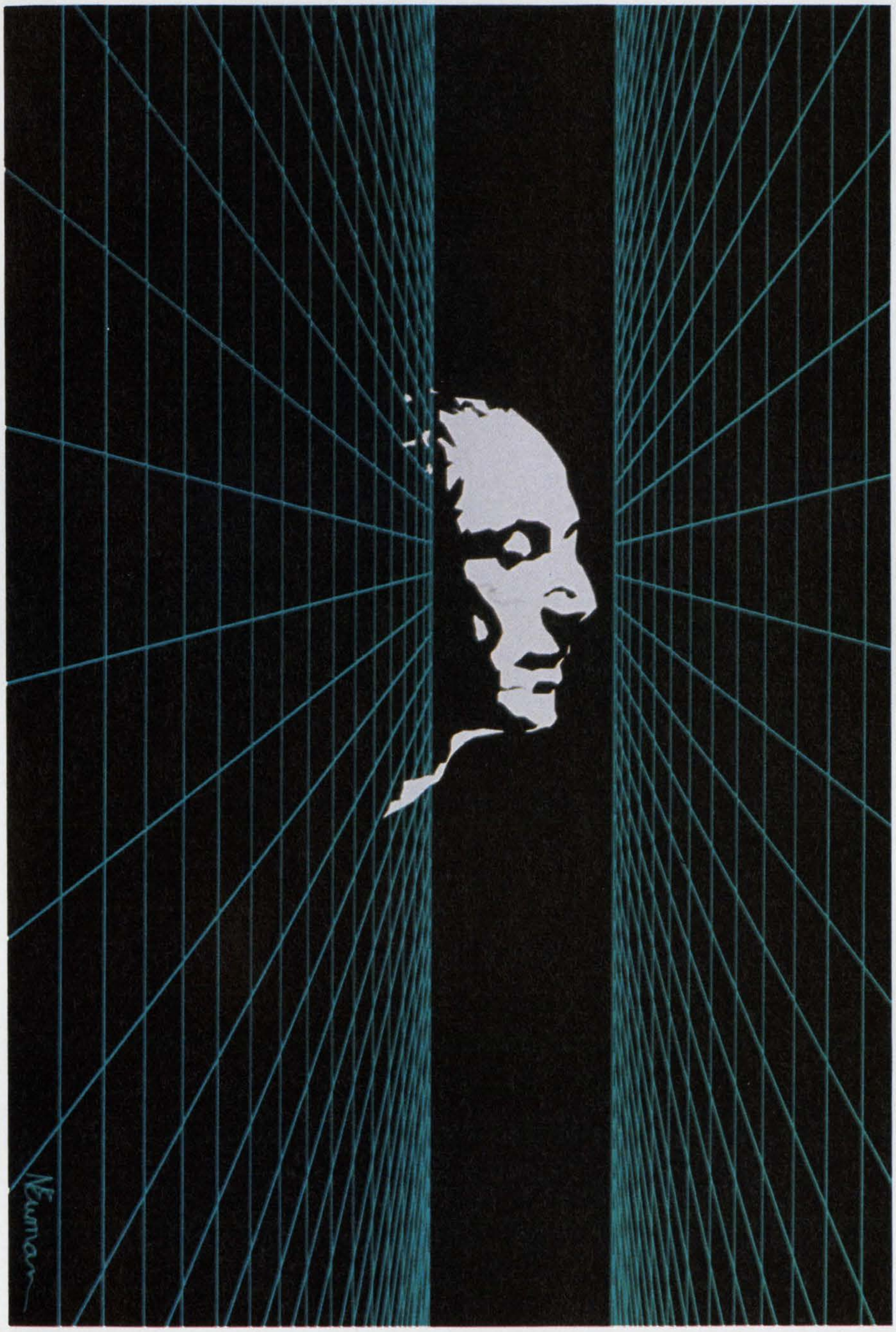

Figure 2: Computer graphics also has applications that are purely artistic, as evident in this composition (courtesy DICOMED Corp).

puter graphics as an instructional aid, both in formal educational environments and in the home; Frontier Applications In Research, covering new applications for computer graphics in a wide range of research areas; Hardware and Software Standards and Directions for the 80s, which will present a host of industry experts predicting what hardware developments we can expect in the near future and what effect software standards will have on computer graphics; Medgraph, a buzzword for computer graphics used in the medical arts; and finally, Petro-chemical Graphics, covering the world of petroleum exploration, the field that represents the leading non-military market for ultra-sophisticated computer graphics.

In a vein related to petro-chemical graphics, Mapping and Cartography sessions will discuss geographic information systems and automated cartography. Two days of classes on University Graphics, while similar to Graphics For Machine-Mediated Learning, homes in on the college environment, dealing with the use of computer graphics as an aid for training engineers and, more broadly, as a tool for a variety of different college instructional programs.

Three full days are devoted to Videotechnology, covering videodisks, videotex, and computer graphics in broadcasting and

Getting The Picture

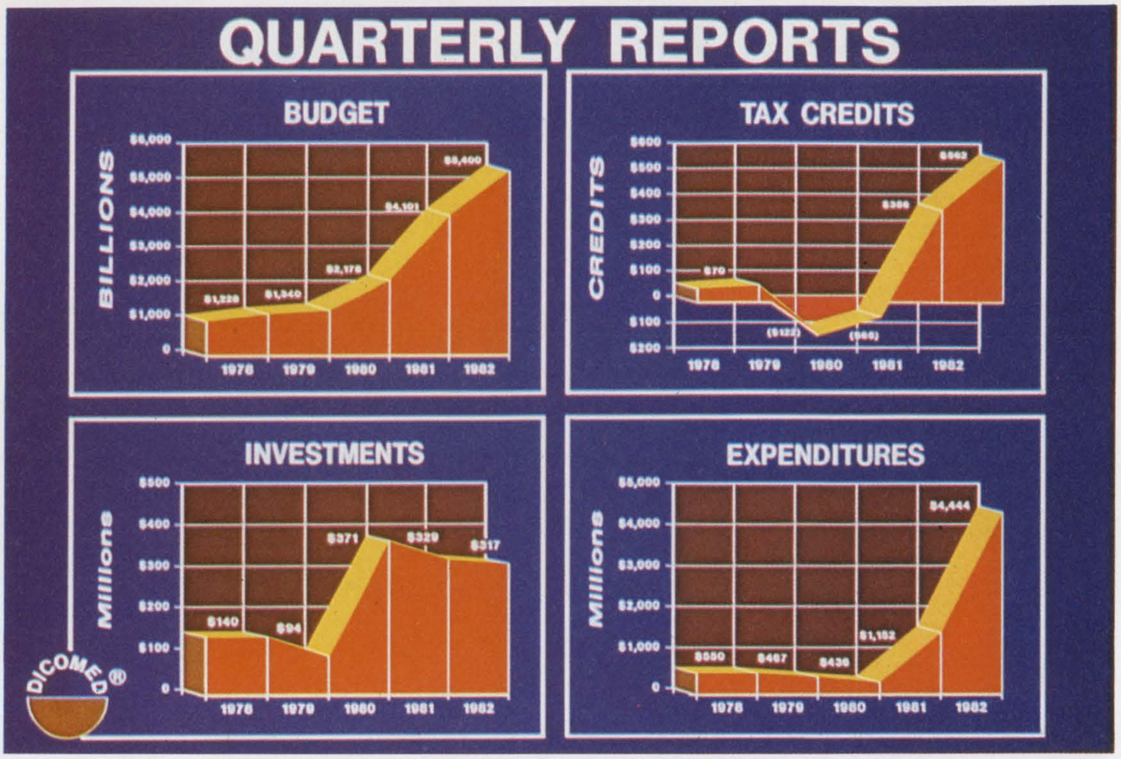

Figure 3: Low cost systems have made business graphics the fastest growing segment of computer graphics (courtesy DICOMED Corp).

cinematography.

One chief use of computer graphics is to turn piles of numerical data into easily assimilable charts. Consequently, Statistical Graphics represents one of the most extensive programs at this year's NCGA. Ten sessions over three days will discuss Graphics And Decision Making, Graphics in Publications, Software For Statistical Graphics, and a number of other topics, featuring participants from the National Science Foundation, the Bureau of the Census, Bell Labs, and a host of other consulting companies, labs and universities.

Low Cost Spurs Applications

The key to computer graphics' extraordinary diversity is its newfound affordability. As a rule, expensive technologies, like computer graphics during the 70s, have specialized applications. As computer graphics systems have become less costly, their practical applications have mushroomed.

Presentation computer graphics is one such application. Now that systems capable of producing charts and graphs for marketing and other business presentations have become relatively inexpensive, this segment of computer graphics, once negligible, has become the fastest growing area in computer graphics today.

Alan Paller, President of AUI Data Graphics and Director of Training and Education for the NCGA, will chair four days of tutorials and technical sessions on Business and Technical Data Graphics. Attendees should be forewarned that Paller describes the experience of listening to one of his lectures as something akin to getting a drink of water from a fire hydrant. And at this year's NCGA, Paller will have good reason to be outspoken: a recent independent study, which Paller will cite at the show, offers the first hard data indicating the benefits of presentation graphics.

Among the study's findings are that meetings using graphics take, on the average, 28% less time than meetings without graphics, people are significantly more responsive to presentations made with graphics, and those who give presentations which use graphics are considered significantly more interesting, better prepared, and more convincing than those who do not. In addition, Paller will discuss what he feels will be the most important technologi-

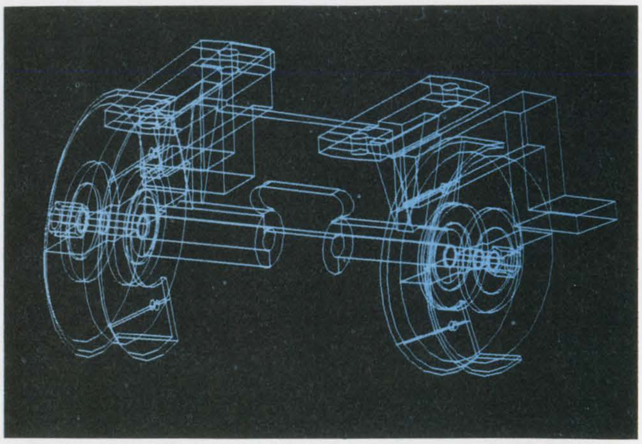

Figure 4: Computer-generated artwork assisting the design of manufactured products comprises a large part of the computer graphics market.

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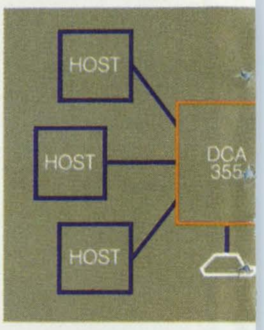

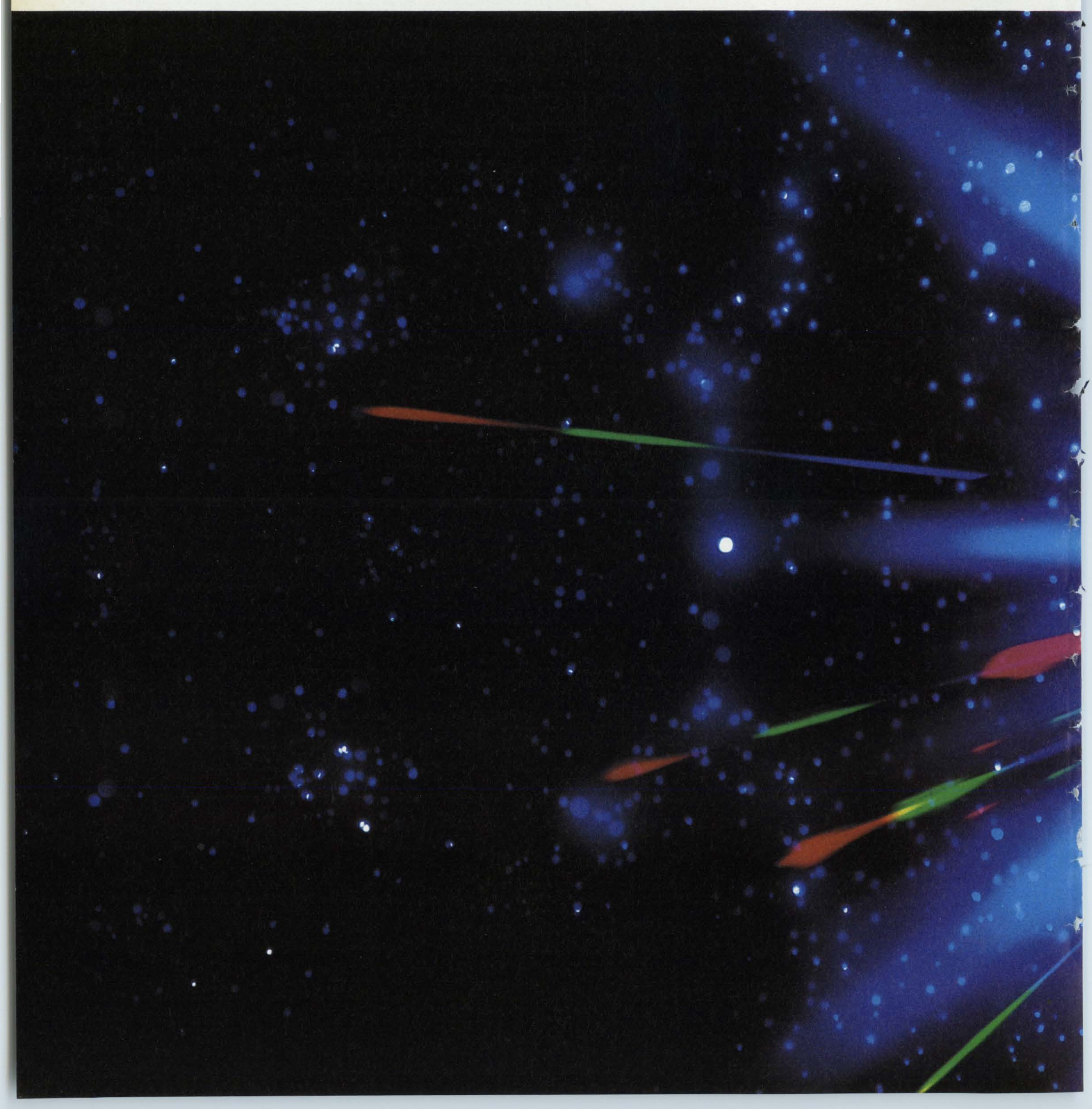

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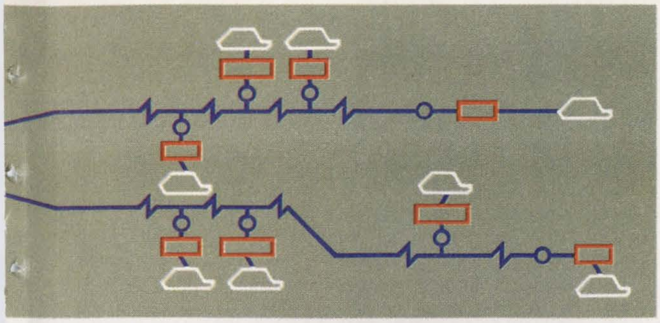

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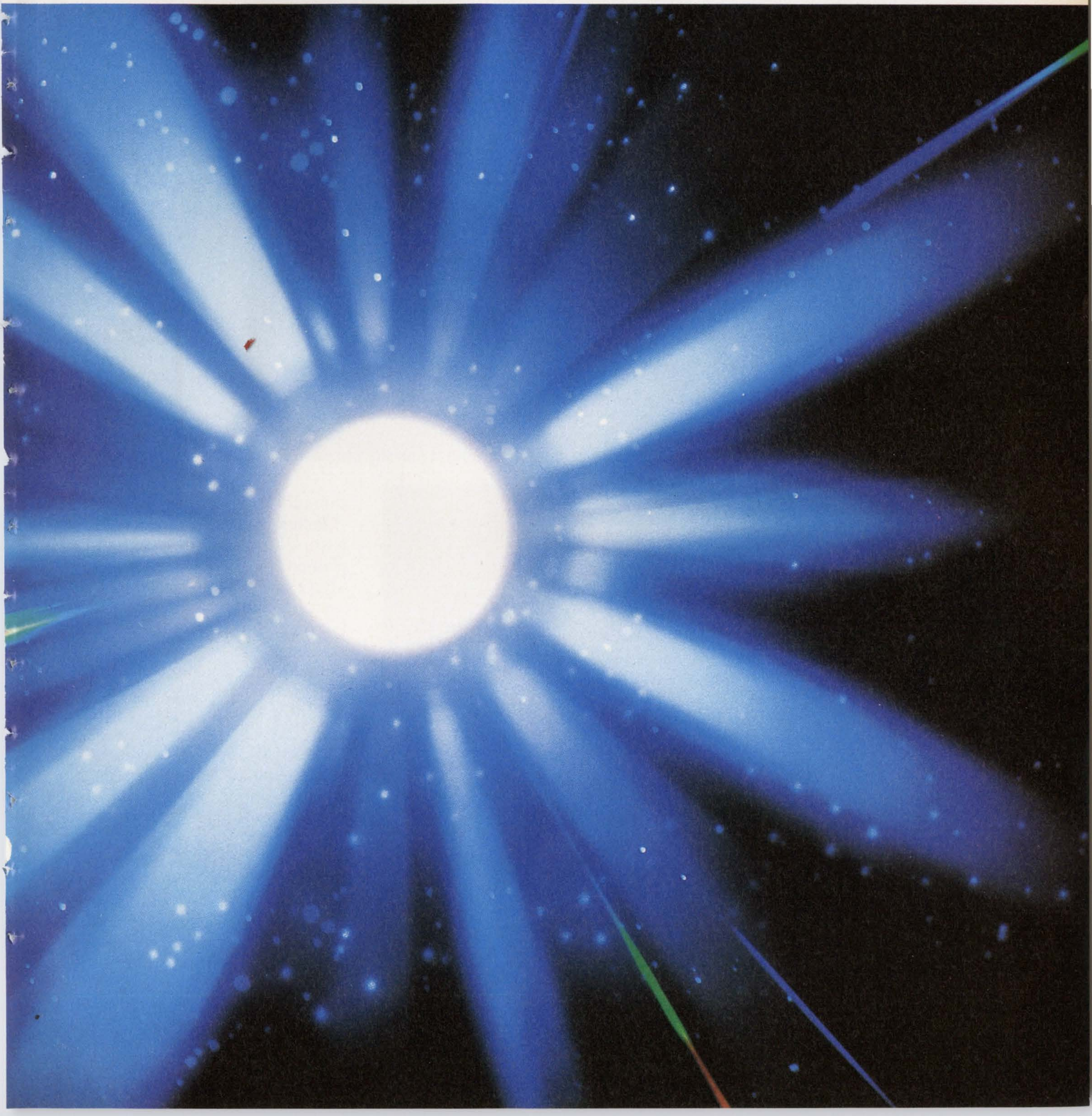

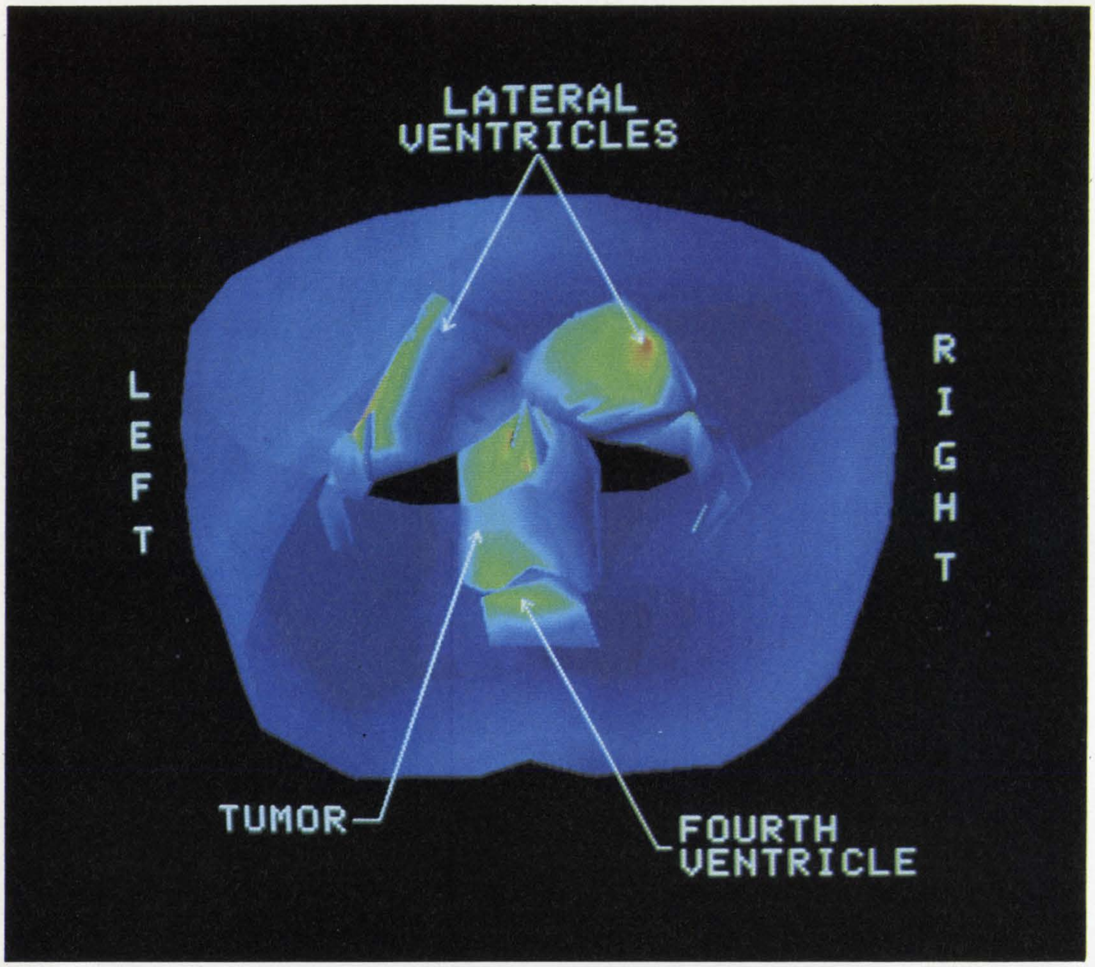

Figure 5: Computer simulation and image processing are invaluable tools for medical diagnosis and training (courtesy University of Kansas Dept of Diagnostic Radiology).

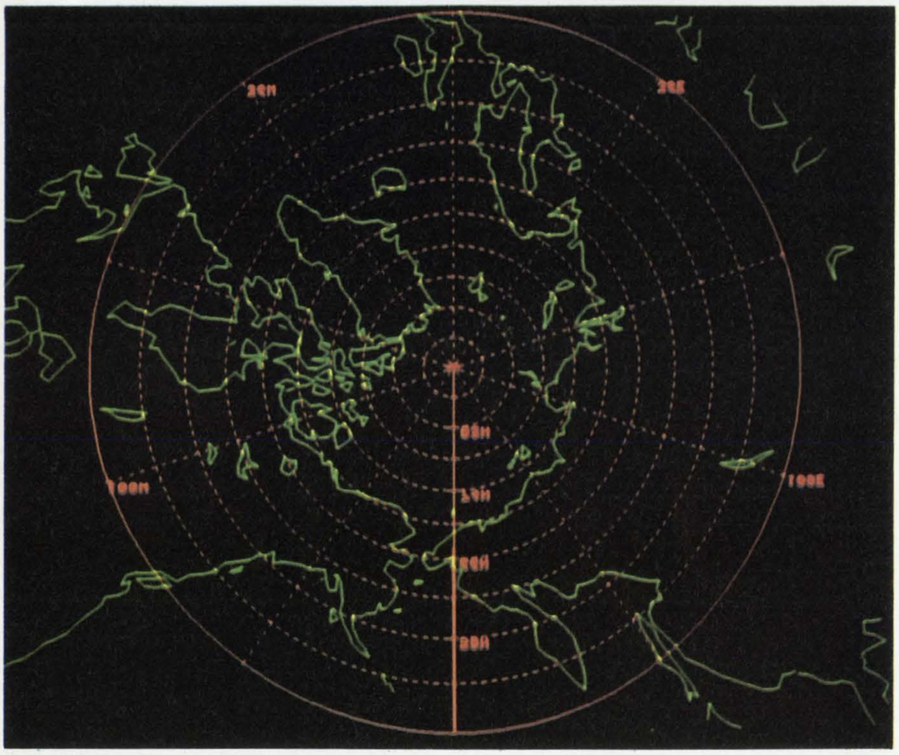

Figure 6: Military applications constitute a large market for sophisticated computer graphics (courtesy of Ramtek Corp).

cal innovations of the coming year.

Paller has been involved with NCGA from its inception, and explained that NCGA began as a SIGGRAPH conference for end users. While working with SIGGRAPH in Washington, Paller says he proposed having some end-users oriented technical sessions. "Their attitude," says Paller, "was 'get away from us—you're dirty.' " After trying repeatedly to find a place in SIGGRAPH for user-oriented sessions, Paller says he gave up, and helped found NCGA, believing there was both a market and a need for a user-targeted computer graphics organization and conference.

Whether or not a consumer oriented show makes as effective an educational forum as a non-consumer show is open to question. But 20,000 attendees and 120 exhibitors leave no question that there is a huge, and growing, demand for NCGA. ☐

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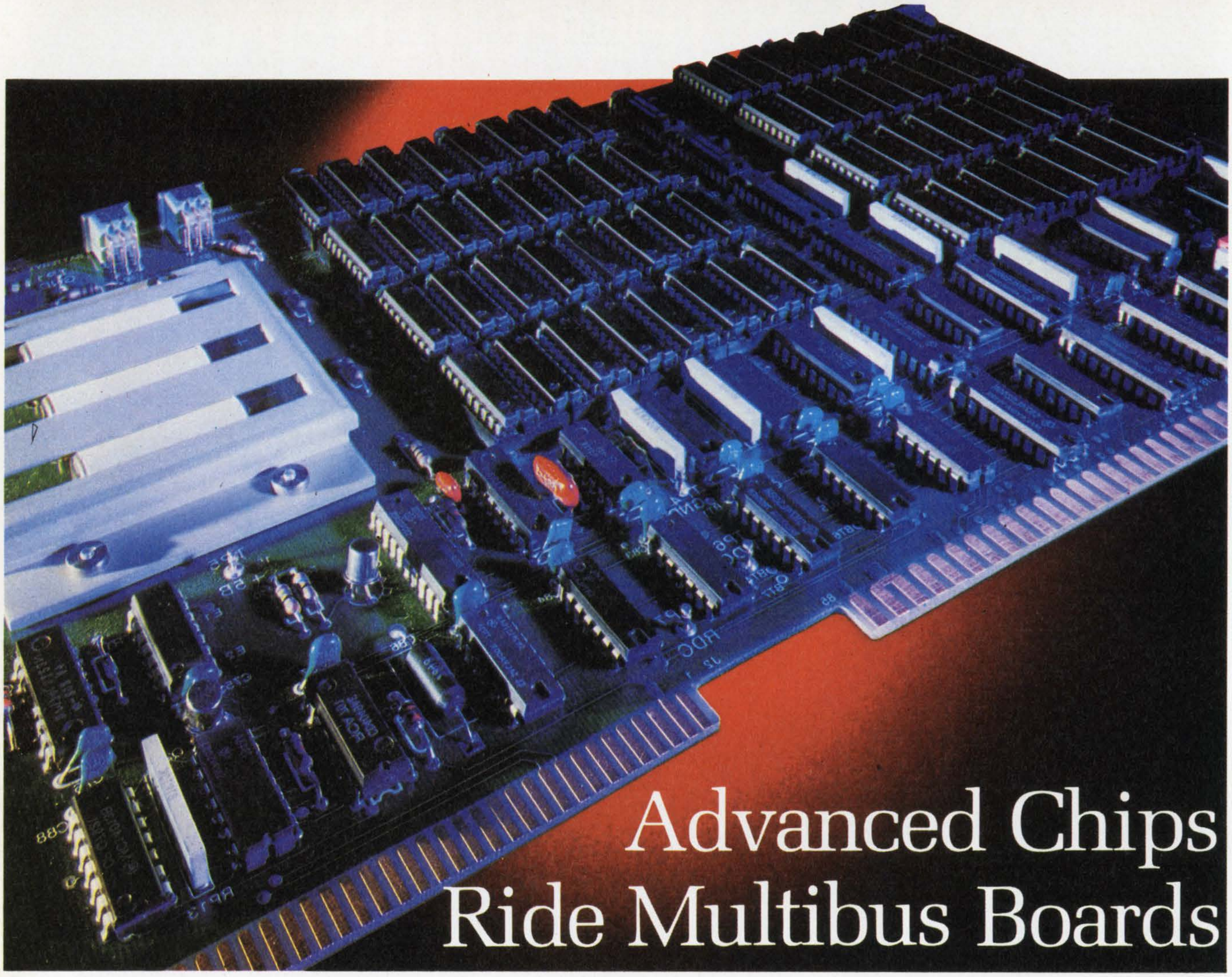

Advanced Chips Ride Multibus Boards

Innovative chips have found their way into Multibus boards and today allow expanded applications

by David Wilson

As the board level designer must constantly keep aware of changes at the device level, so the systems integrator must also appreciate the role of these circuits in the finished design. With this understanding, he may more fully understand the capabilities of the final product and the advantages he can glean from any innovation.

This article addresses both the board level designer and the systems integrator. It will review the latest products to reach the editorial department of *Digital Design,* as well as interpret the advances that have been made. We have broken down the various board categories to aid the reader in his task.

Memory Boards

While browsing through the catalogs of Multibus memory manufacturers, the reader will note two distinct types: Integrated Circuit Manufacturers (such as Intel and Texas Instruments) who stuff a board with their own parts, and the Independents, such as Ikier and Stynetic Systems, who design around a number of different IC houses' products.

Stynetic Systems Inc, has introduced a memory board, the NVR8010 (**Figure 1**), which uses "shadow memory." "Shadow memory" is a concept pioneered by Xicor Inc. (Milpitas, CA). Their X2212 part **(Figure 2)** contains 2K of memory organized as a conventional 1K static RAM overlaid bit-for-bit with a non-volatile 1K Electrically Erasable PROM (E^2PROM). Non-volatile data can be stored in the E^2PROM and at any time, data can be transferred back and forth between the RAM and E^2PROM by simple store and array recall signals. To add to the device's flexibility, high voltage pulses or supplies are never required. A single 5V supply is the only power source required for any function.

This Stynetic board is the first in a series of non-volatile memory board products the company is introducing in 1982, all of which utilize the features of non-volatile, high-speed RAM without the need for batteries or backup of any sort.

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The application areas in which the NVR8010 has found use include industrial control systems, automatic test equipment, CRT terminals and data communications devices, according to Jeffrey Stein, President of the New York-based company.

More specifically, the board has also been used in disk-based systems to act as a non-volatile buffer for information *before* it is placed on disk, so that such information is never lost even if power fails during a disk write operation.

The board itself provides 8K bytes of high-speed, static RAM and 1K byte of battery-less, non-volatile "shadow RAM." The non-volatile RAM is fully speed compatible with the static RAM and totally transparent to programs in all operating modes; in short, it appears to the host system as traditional RAM memory. Via simple jumper straps or the board, the 1K byte non-volatile memory block can be logically inserted into the addressing decode structure to occupy any of the eight 1K byte blocks of memory implemented on the board. Non-volatility is then provided transparently to all other system operation.

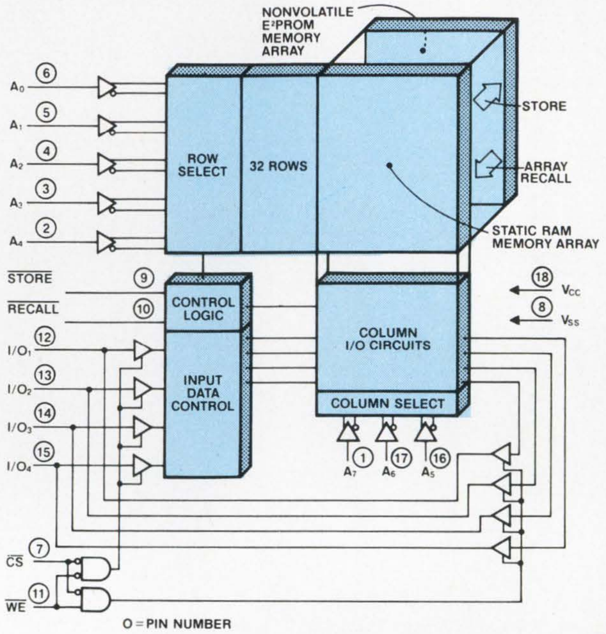

Figure 2: Functional diagram of X2212 (256x4) which contains 2K of memory organized as a conventional 1K static RAM overlaid bit-for-bit with a non-volatile 1K E²PROM.

Error Detection and Correction

The increasing density of semiconductor RAMs has brought with it the well-publicized problem of random soft errors due to alpha particles, and hence the need for error detection and correction.

Two distinct approaches have emerged to tackle the problem. First, the CPU board may be used to handle the task, or alternatively, specialized EDC chips may be placed on the memory board. Over the past few years, the IC houses have addressed the problem by introducing a variety of Error Detection and Correction devices. The idea of localizing the circuitry on the RAM board is a technique that eliminates the high software overhead of the former approach.

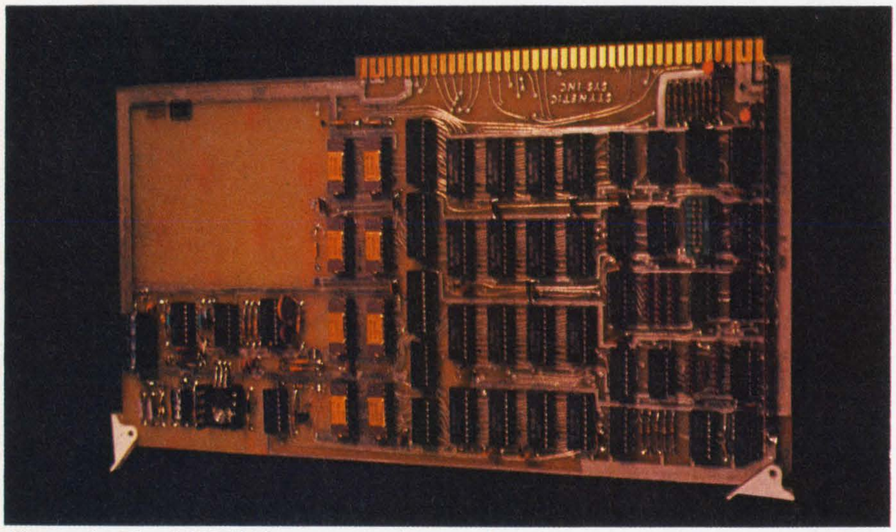

Figure 1: The NVR8010 is a recently introduced Multibus board using "shadow memory," a concept pioneered by Xicor.

Some companies claim that error correction significantly increases the reliability of a memory system, and calculations from several manufacturers indicate that single-bit error correction can produce between 50 and 80 times improvement in reliability.

Advanced Micro Devices, a manufacturer of both integrated circuits and Multibus memories, has recently announced plans to incorporate its own EDC device onto its board level products, an approach that Texas Instruments has already used in its designs.

Other manufacturers of Multibus memory boards are claiming that, for some applications, as the 64K learning curve falls, the memory devices themselves are reliable enough without EDC, and that EDC devices only slow up the access time of the board.

Graphic Boards

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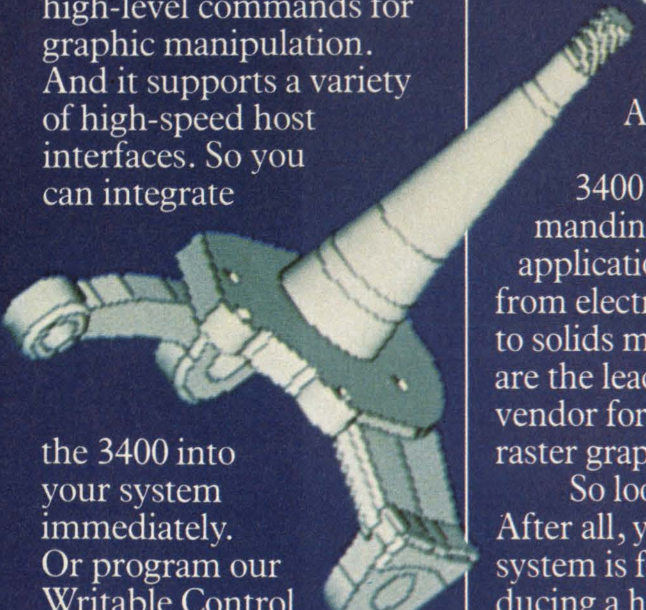

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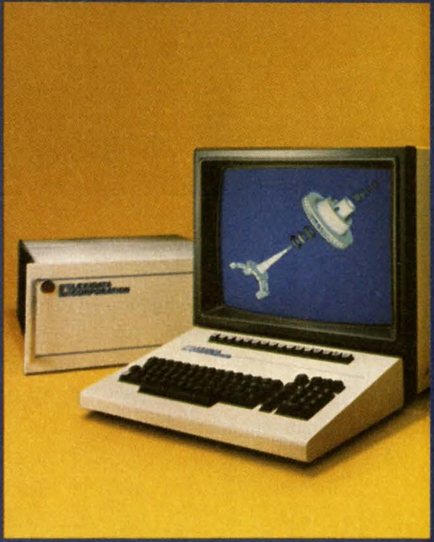

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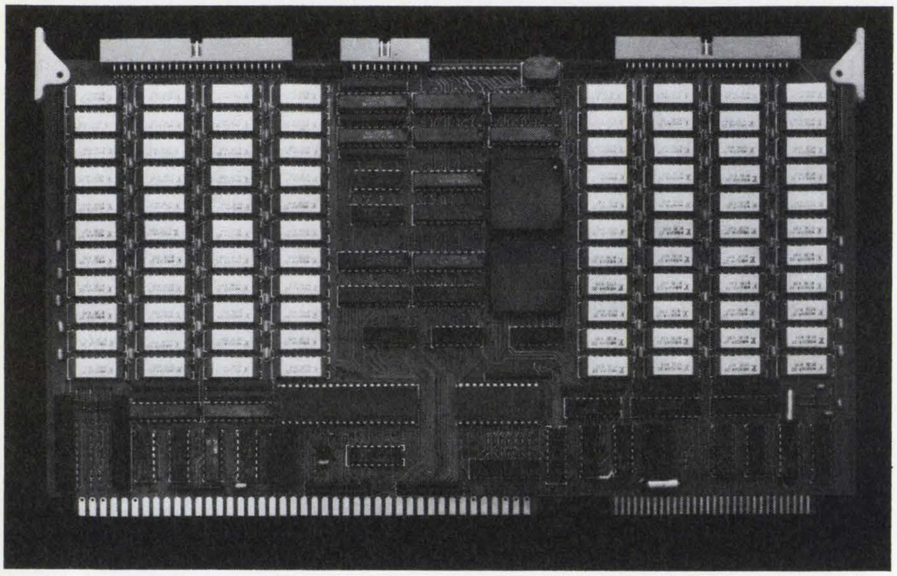


Figure 4: ADT's very large scale, high-speed Multibus memory features memory management and error detection and correction.

supporting a high resolution board with a reasonably priced monitor.

In systems design, farming out intelligence to peripheral boards appears to be a common trend, freeing up the CPU card and increasing system performance. Let us look at a typical system from Ikier Technology, a recent start-up company in Burlington, MA.

The key to the system **(Figure 3)** is the video controller designed around the latest NEC device, the μPD7220. Like other controllers on the market, certain tasks are executed without the aid of the central CPU card such as, the refresh of on-board RAM and the accessing requirement of the CRT.

In the Ikier design, the programmer's task has also been simplified in that less complex software statements from the CPU card are required to select memory segment for display, to pan and scroll or to zoom up to 16X magnification. These commands also enable lines, circles, arcs and rectangles to be placed in memory. Other commands can perform automatic update, complement or set and clear operations on a selected memory segment.

More Complex Tools

One of the problems faced by today's integrator is the development of a system that will support a number of users executing a variety of tasks.

To achieve the design, a very fast large memory with memory management will need to be specified. **(Figure 4).**

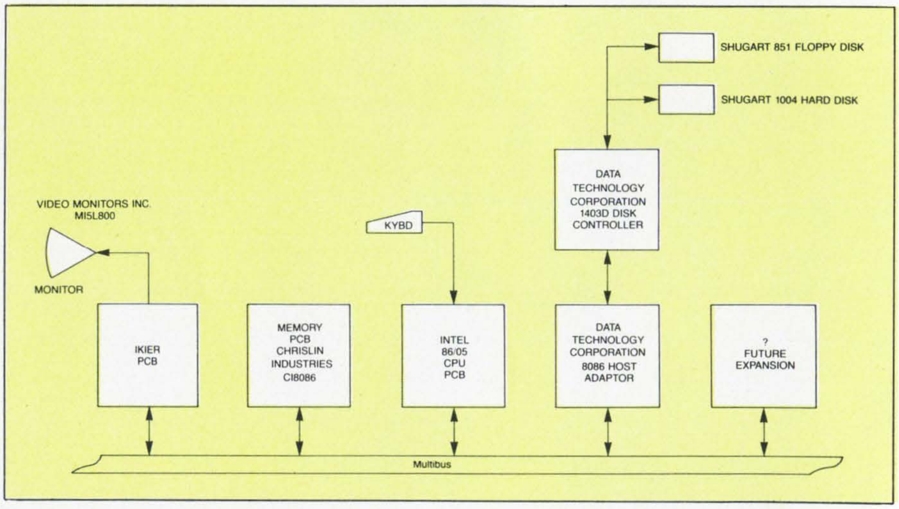
Advanced Digital Technology's latest memory offers capacity of up to 1.5 Mbytes in 128K byte increments, and the memory is specified at 250ns access time and 440ns cycle time, thus reducing the wait states in currently available Multibus memories, according to ADT.

Typical computer system difficulties of program partitioning, resource sharing and memory fragmentation were the design considerations behind the board, that also provides the functions necessary to implement a cache memory for floppy and Winchester disk systems.

The ADT memory systems are supplied with addressing and allocation features that provide the user with dynamic memory mapping, paging and segmentation throughout the 16 Mbyte range. Starting addresses are provided on contiguous and non-contiguous 16K byte boundaries. These features support systems with 16, 20 and 24 bit address buses. The system permits an 8-bit processor access to 16 Mbytes of memory with a 16-bit address bus. The system also allows the user to dynamically swap multiples of 16K byte segments in and out of the processor space. System programmers may use these features to enable programs with different segmentation requirements to reside in the system. The virtual addressing aspects of the system permits multiple processors to access re-entrant routines.

Racking The Cards

Physically, Multibus-type printed circuit board (PCB) cards are 12″ long, 6.75″ high and less than 0.6″ wide. Two connectors, P1 and P2, are specified for connecting the printed circuit cards to the Multibus. Connector "P1" commonly called "the Multibus" is an 86-pin dual-sided edge connector with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INTEL 86/05 CPU PCB
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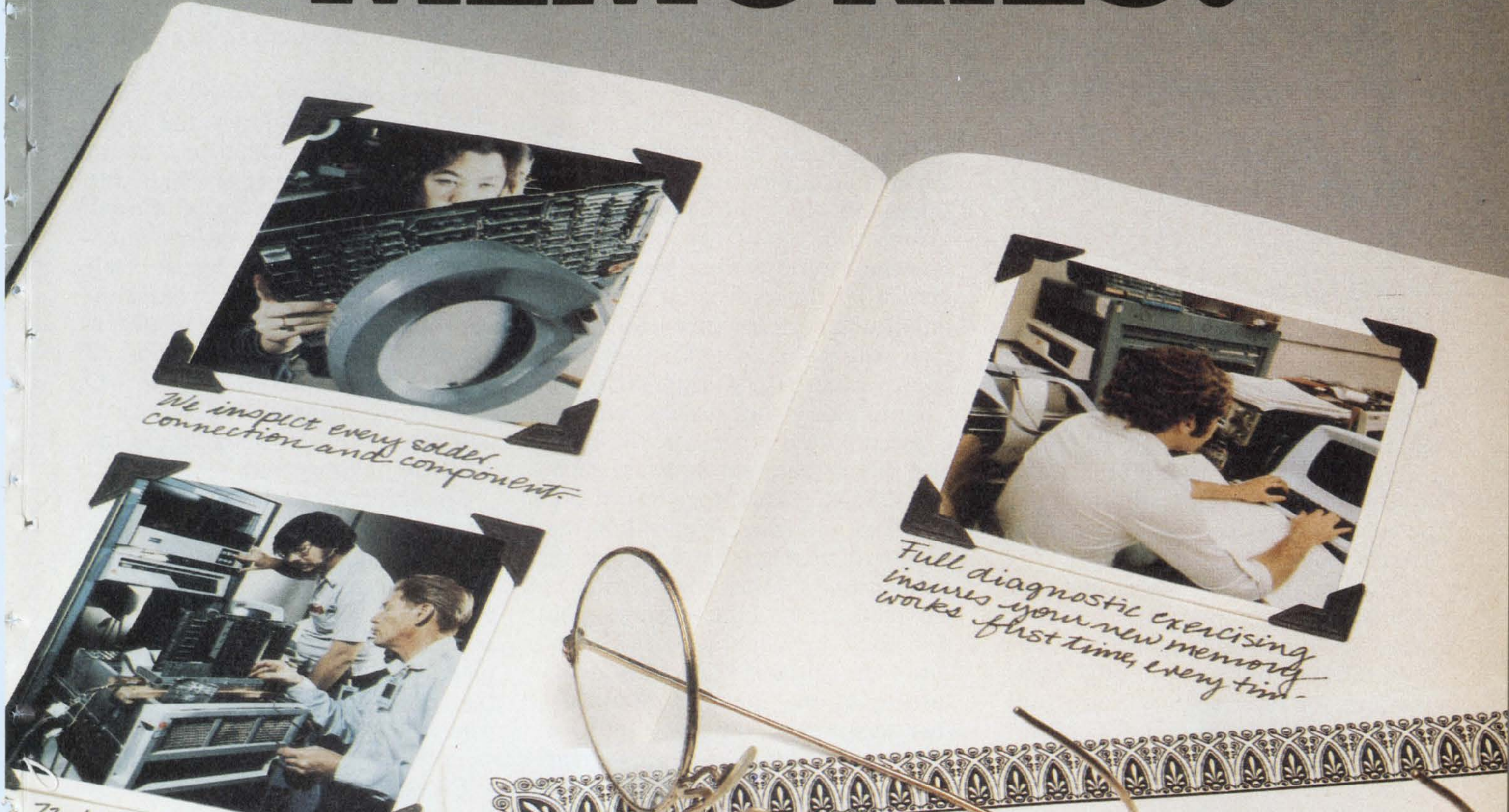
Figure 3: A typical graphics system from Ikier Technology uses their video controller board designed around the NEC μPD7220.

LASTING MEMORIES.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Often the user is faced with problems for which off-the-shelf solutions are unavailable, such as interfacing to the outside world.

0.156″ centers; it is the primary interface with all signals defined by pin number. Connector P2, with signal undefined, is a 60-pin dual-sided edge connector with 0.1″ pin centers which is used as an auxiliary interface.

The non-bus (top edge) side of a Multibus compatible PCB can contain various combinations of 26-pin, 50-pin and 100-pin edge connectors for interfacing to serial and parallel I/O devices, CRT terminals, floppy disk drives, and sensors.

Simultaneous with the design of hardware and software systems, some thought must be given to the choice of card cage or chassis dimensions that the above boards reside in. At present, with the proliferation of NMOS μPs and memories, the designer is obliged to choose a cage that includes a cooling fan, such as the Am 95/6440 from Advanced Micro Devices. Already, however, boards are available with 8-bit CMOS processors such as Diversified Technology's (Ridgeland, MS) NSC800 board, and it seems only a matter of time before the recent Intel/Harris agreement bears fruit with an 8086 16-bit CMOS part. As well as consuming less power, these boards will make the use of cooling fans redundant in many systems designs.

Floppy Disk Controllers

The role of floppy disk controller (FDC) board is to provide an interface between the drives and any Multibus system.

Essentially, there are two approaches that have been taken in board design. Either data may be put directly onto the bus, or it may be stored in a buffer memory on the board itself. The first approach is suited to a low cost system where the user may be unconcerned about tying up the bus for a long period of time. In situations where systems resources are a prime consideration, the latter approach is taken, and many of the newer boards are offloading system demands by the use of an on-board intelligent peripheral controller. A typical example of this sort of board is the BP2190 from NEC.

Once a disk transfer has been requested by the processor, the FDC and direct memory access controller (DMAC) work together to obtain data and transfer it to/from the on-board memory through one of its dual ports. When the transfer is complete, the FDC notifies the processor by generating an interrupt. The on-board dual port architecture of the memory allows either disk data transfers to take place under DMA control, or for the host processor to have access to the memory. All disk data transfers occur between the drive and the on-board RAM.

Interfacing To Outside World

System design headaches are usually not simply restricted to choice of Multibus cards and design of system software. Often, the user is faced with a unique set of problems where off-the-shelf solutions are unavailable. One of these problems is interfacing systems to the outside world.

Some companies, however, have made inroads to address the problems. Like other Multibus board designs, some designs, like the RMB-741 from Robotrol Corp., contain a μP that controls interface operations. The board itself provides 12 completely independent analog outputs and 16 differential or 32 single-ended inputs, all with 12-bit resolution. The bus I/O is memory mapped and is selectable to any 16 byte boundary in the 1 Mbyte memory map.

Six different modes may be programmed by the host CPU. The analog inputs may be jumpered for either differential or single-ended operation. The A/D conversion section contains a sample-hold amplifier and a variable gain amplifier that is software programmable for gains of 1,2,4, and 8. The A/D sample rate is 23kHz.

Each D/A output is separately configurable for a voltage or current loop output, and several jumper selectable voltage ranges are available. The 4mA current offset for the current loop may be directly generated by the hardware, by the on-board μP, or by

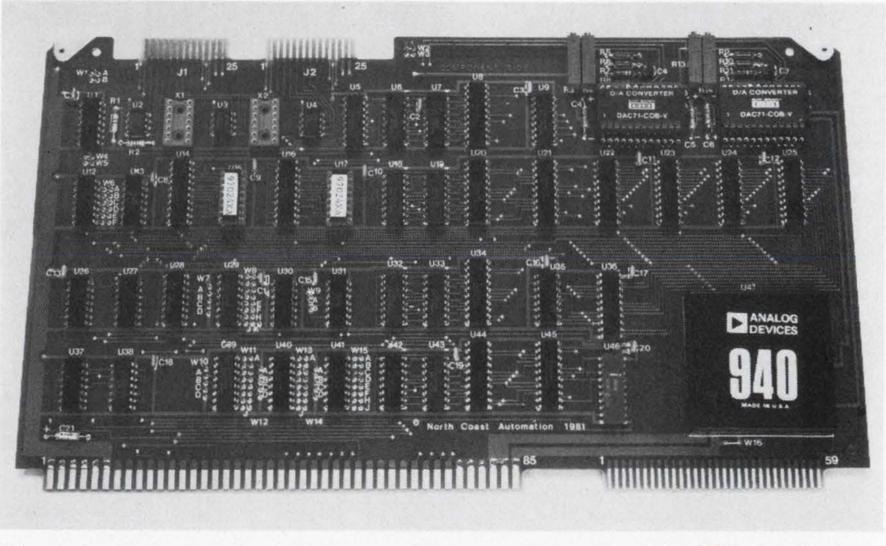
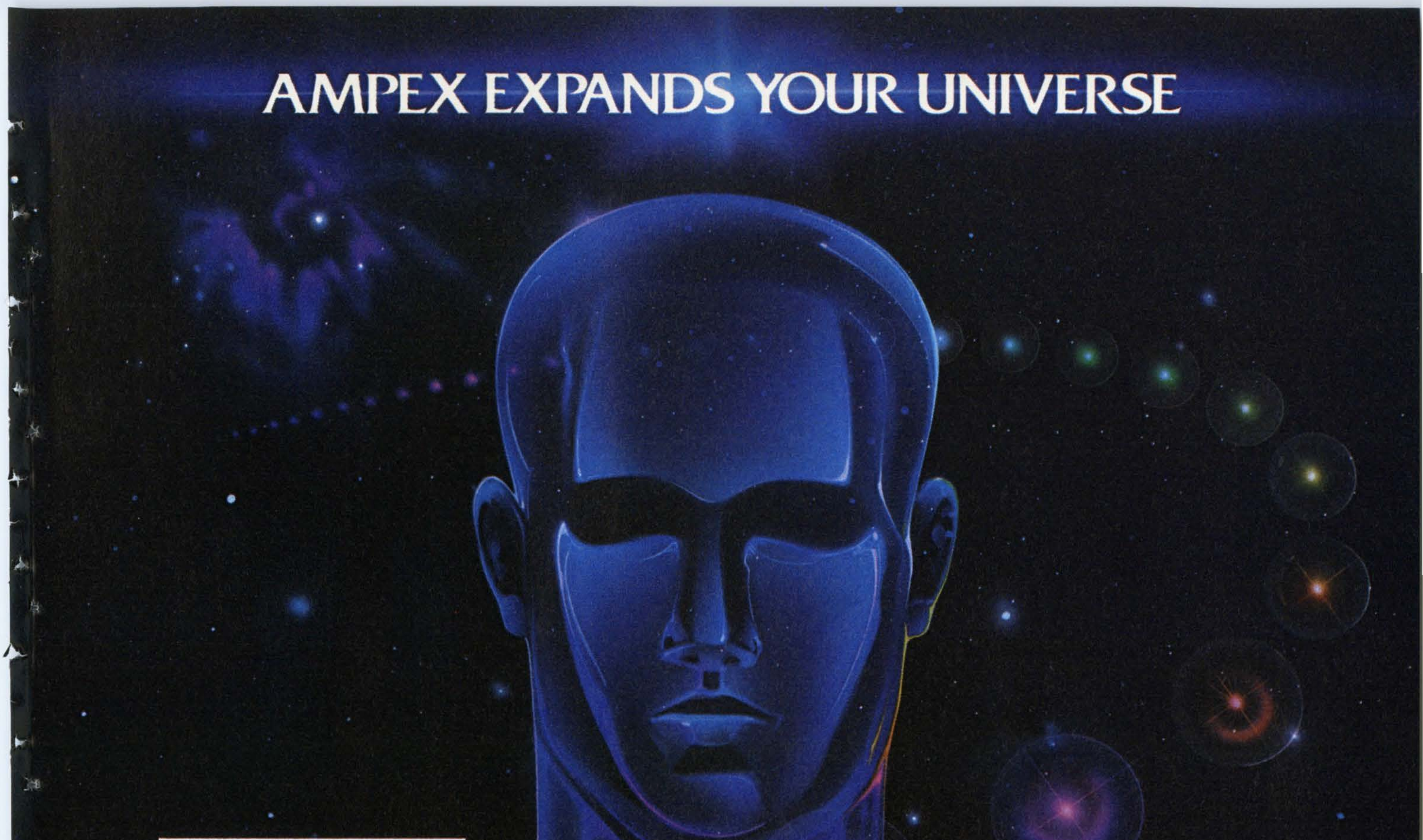


Figure 5: Accepting signals from two incremental encoders, the 9702 family from North Coast Automation combines incremental encoder and D/A computer interfaces on a single board.



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the host CPU.

In application areas such as machine tools and rolling mills automation, it is necessary to interface the Multibus to motors. The 9702 family from North Coast Automation **(Figure 5)** provides a combination of incremental encoder and digital-to-analog converter interfaces on a single board.

All boards in the series accept input signals from two incremental encoders. Each encoder interface consists of decoding logic, a status register, a marker latch register and a 16-bit counter. Optionally, the series can be equipped with two digital-to-analog converters to produce voltages for driving motors based on commands from a μP. An inexpensive μC can use this interface board with its 16-bit D/A converters to provide the resolution required in precision position and velocity control. For less demanding applications, 12-bit D/A converters are available. Both versions are available with DC/DC converters for the ±15V supplies required.

Check It Out

Fast, electrical checkouts may be required when the user first installs his D/A board. One way of doing this is to use a diagnostic program on a floppy disk that can be used to calibrate the board when the input format or output range is changed, or as a routine calibration program. Such programs are currently available from some vendors, and the prospective designer should check out this field before committing to his purchase.

There are six main functions of the diagnostic program currently available from Datel Intersil to check out its 8-channel, 12-bit D/A output board, the ST-728: calibration and sawtooth tests, the calibration table, set base address, exit and help. These tests include checking missing or shorted bits, and permit the user to enter the base address of the ST-728 D/A board without reconfiguring the board's base address.

Further Reading

The reader may be interested to note that a new up-to-date buyers guide lists more than 500 Multibus compatible board level products from over 90 manufacturers.

The guide also lists local sales offices and distributors in addition to the Multibus compatible product listing. Purchase of the guide also includes new Multibus product announcements between issues.

The Multibus Buyers Guide is published twice a year and is available from the publisher: Ironoak Co., 3239 Caminito Ameca, La Jolla, CA 92037; (714) 450-0191. $19 first copy, others $8.95 each.

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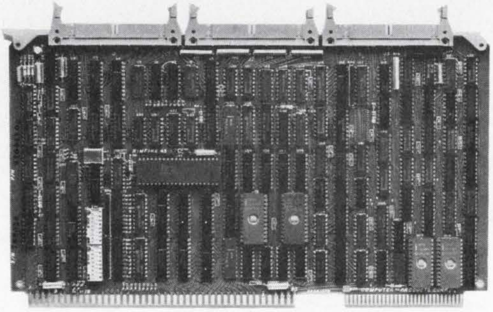

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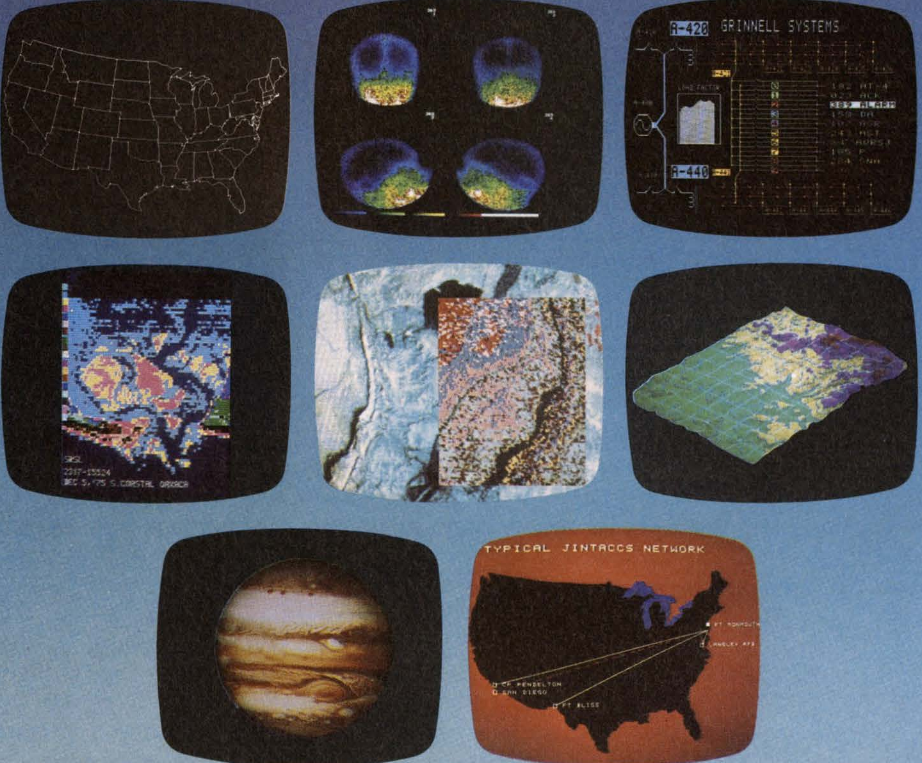

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Designer's Guide To Keyswitches

by Paul Snigier

The rapid growth of low-cost consumer and industrial electronics has created a demand for inexpensive computer input devices, especially keyboards and keypads. These keyboards/pads fall into two categories: contacting and noncontacting. Contacting switches include membrane, sealed reed, crossbar and related categories. Noncontacting types include saturable core, photo-electric or -optical, capacitance coupled and Hall-effect units.

> *Data entry is seeing a number of changes relevant to designers, the most important of which may be the growing confrontation between membrane and capacitance switches.*

Hall-Effect Keyboards

Cadillac quality at Rolls Royce prices make Hall-effect keyboards suitable for high data-input uses. Not only are they rugged, but they offer advantages of long life and bouncelessness. A plunger has one or two magnets, which are mounted on either side of a "prong" that pushes down past an IC chip. Each IC requires 10 mA of continuous current. The Hall-effect eliminates bounce, once a worry that has now been reduced to near triviality by the μP and low-bounce (100 μs to 300 μs) switches. It is a technology that is declining in popularity, due to price.

Saturable Core Ferrite Keyboards

In saturable ferrite-cored switches, magnets on the plunger straddle a ferrite core, saturating the core whenever the keytop is pushed, thus pushing down the plunger. This inhibits drive-to-sense winding magnetic coupling. Like the Hall-effect switch, saturable core switches are costly; and, with lowered membrane and capacitance switch costs, and their rising reliabilities, saturable core keyboards may slowly become obsolete.

Hard Contact and Reed Switches

Hard contact switches move one gold-plated bar past another at right angles (cross bar switching), so that the small knife-edge contact area (9×10^{-6} in^2) will create high contact pressures (5 kpsi). An operating cam and spring cause the plunger and keycap to rebound.

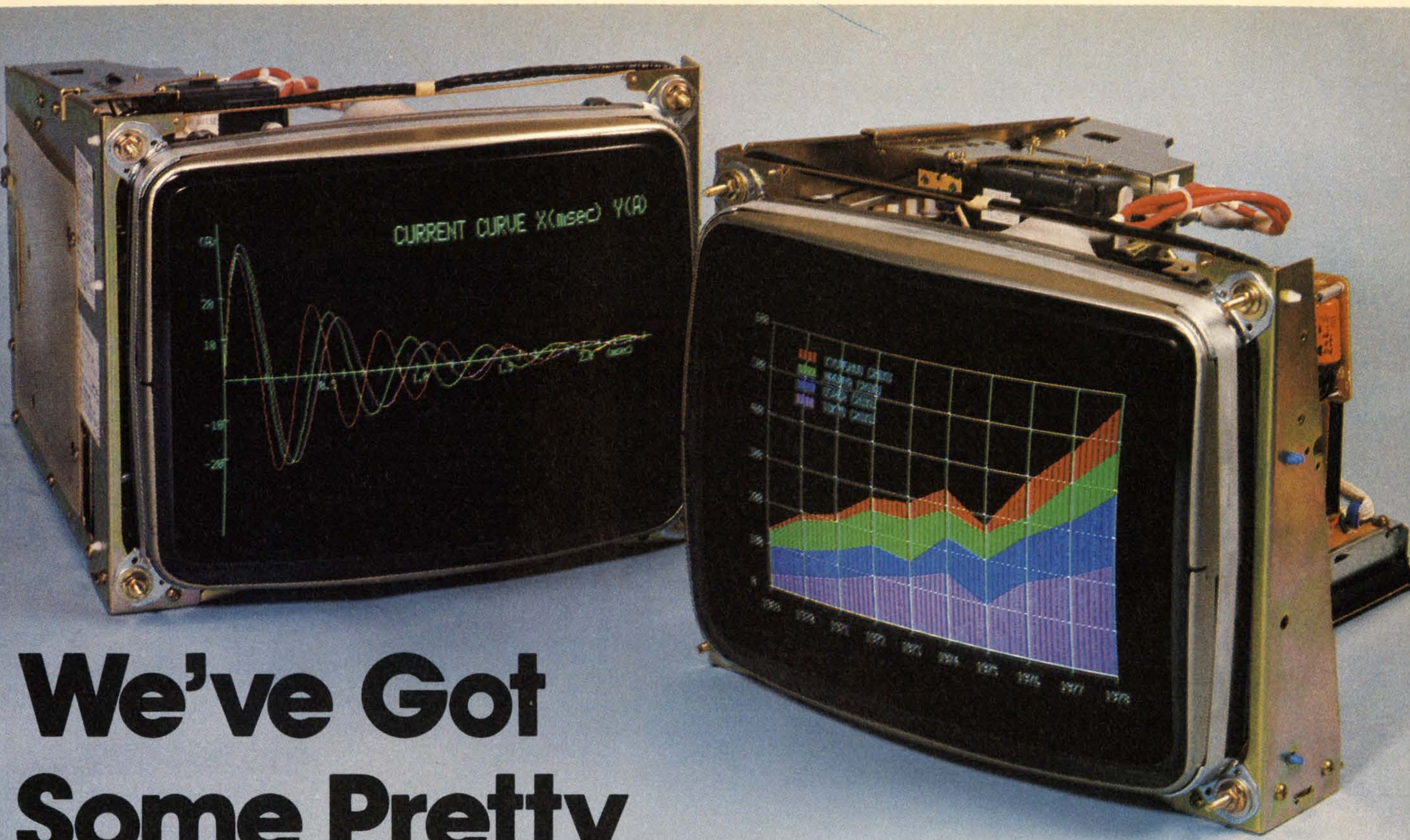
On the reed switch, the keycap and plunger are attached to a toroidal-like permanent magnet that is pushed down past the reed relay causing the normally open reed blades to close, until the keycap is released. The reed relay switch relay is hermetically sealed, so it is immune to contaminants.

In mating, contact switches may be butt, wipe, or both. Wiping contacts may give lower contact resistance by removing and penetrating surface contaminants, due to poor wave soldering, fluxing and cleaning, or from oxidation (nonconductive surface oxides and sulfides) and particulate matter. However, wiping action (if strong) can wipe off a 10-μin gold flash as well as contaminants. Unlike butt action, wiping can delay interrupting the current, creating microarcing. This cuts switch life and raises contact resistance, not to mention RFI generation. Thumbwheels have lighter wiping and double-wipe rotaries have quite vigorous wiping, which is the reason why they have such low contact resistance. Some rotary tape makers have overcome this obstacle by using large contact studs, across which the ends of parallel contact spring leaves brush.

Although mating is quantifiable, physical "feel" is not. It is partly a matter of operating force. This is doubly true with multiposition switches (like thumbwheels) or rotaries. If you have operated a thumbwheel that "rolls" past where it should stop, then you understand the problem. A two-position rotary foils fumbling, as does a key-operated switch. The ultimate, however, is to install a hinged hood over the switch, perhaps even locking it shut.

The problem of "feel" is an obstacle for small switches, which don't have room for an adequate spring or detent action (where it seems to fall into one of several equilibrium or stable points). However, don't just settle for feel. Tactile feedback is paramount, but don't neglect the auditory feedback of a good, solid click. Many have it; and, if not, some vendors design it in. Specified within wide limits, torque can worsen as the mating surfaces wear, as lubricant is lost and as bearings go bad.

Reliability is affected by switch housing, and an open, closed or fully-sealed switch may be needed. A corrosive or humid environment will require the fully-sealed switch. If an end-of-life maximum contact resistance is specified, and a cheap



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insulator in it absorbs moisture, the switch may still meet end-of-life values, but the excessive inter-contact leakage current will make the question academic. Of course, improper wave-soldering can work up tiny solder, flux or solvent. Sealed switch bottoms may not be enough; a top removable seal may be needed. Ask to see dye/UV testing results if this is a worry.

Transients can vaporize gold flashing and expose the contact base metal. Gold is intended for low-level loads, so it should not be used even momentarily for higher-level loads. Gold is not plated evenly, so that some contact microareas will have greater current flow and heat up more.

Photo-Optical Advantages

Photo-optical switches offer advantages over many contact and non-contact (including semiconductor) categories, including fewer moving parts and resulting reliability gains.

One keyboard was introduced last year by Optical Techniques International of Santa Ana, CA. Its visible light, flat-top keyboard was recently augmented by an IR version that consumes less power and is more reliable (IR LED emitters and sensors are four times more reliable than visible spectra devices). And, now that power consumption is low, partly due to lower-parts configurations, this previous obstacle has been minimized. In OTI's keyboard, one LED-sensor pair handles an average of three keys. The average keyboard will draw 250 mA.

Since LEDs are omnidirectional emitters, detectors can sense the absence of the light-beam blocked by a plunger. A single LED and several detectors create a spoke-like beam pattern. The six keys around it can interrupt it, while those two keys that are three-levels away are decoded by the beam and a second beam from a second, closer LED. An 8048 decodes these interruptions into ASCII. LED rise-times of 8 ms permit turning LEDs on and off 50x/s which saves power.

Although IR LEDs are more reliable, they can still fail. OTI uses a self-test diagnostic routine that tests components upon power-up. Upon failure, keys can easily be separately snapped out. Plungers do not touch the PCB, and key life is 100M cycles.

Burroughs of Detroit, MI, will offer dp-type photo-optical keyboard terminals; Motorola sees a bright future for its invisible IR LED emitters/sensors. They now cost 80¢ to 90¢ per key in quantity, but may never fall down the learning curve as fast as other types.

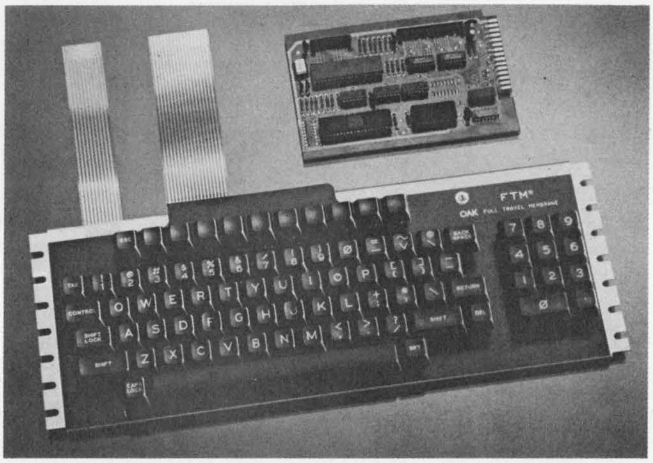

Figure 1: Full travel membrane alphanumeric keyboards combine membrane's low-cost reliability with human-feel, full-travel plastic keyparts, pretravel, and hysterisis. This 81-key FTM keyboard is available from Oak Technology.

Capacitive Keyswitches

Capacitively-coupled keyboards provide one of two designs. In the traditional design, a moving plate at the bottom of the plunger moves down into the surrounding foam cushion, coming closer (but not touching) two PCB-mounted pads connected to two switch terminals. Later (Digitran) units dispensed with the foam and plunger plate and pushed a hinged moving plate closer to a fixed PCB-mounted plate, thus closing the plate-to-plate distance and raising capacitance. Upon releasing key top pressure, the hinged plate pushed the plunger back up. This helped solve the problem of deteriorating sponge foam cushions that altered capacitance when they absorbed moisture.

Although initial capacitance switches once actually used AC, pulse techniques are used now.

Earlier capacitive switches were susceptible to EMI, RFI, static and poor layout. Low switch capacities, typically a few pF, were no help. In addition, the small signals required better sensing. Finally, the keyboards, despite "umbrellas" and hoods, still were essentially open to invasion by contaminants.

Low initial cost, reliability, and the absence of precious metals contributed to capacitance keyboards' immense success. Lower assembly costs are due to the need not to solder each keyswitch to the PCB. Isolation diodes are not needed on each keyswitch for n-key rollovers and other functions. The no-gold, no-silver advantage is due to the switches no-contact quality.

Membrane Switches

Membrane switches specifically interface to electronic logic where large push button arrays are needed at low cost. Full-travel membrane (FTM) keyswitches are now providing tactile feedback, once an objection to their use in high data input applications. Further FTM developments may soon see newer FTM keyboards that will erode Hall-effect, capacitance and other contact/non-contact keyboards in dp-type applications.

In construction, the membrane switch is simple; it consists of a sandwich of three, thin insulating films. One forms a front layer, with an inner surface upon which are deposited movable contacts. On the rear film stationary con-

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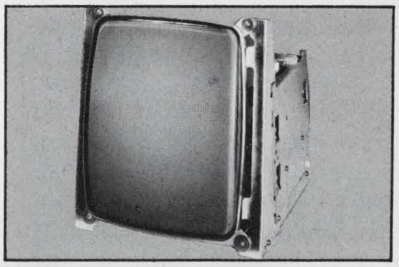

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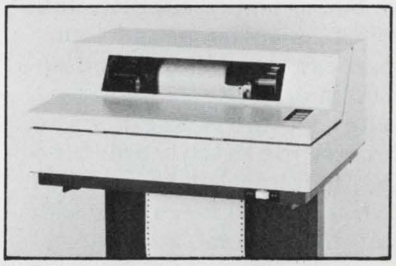

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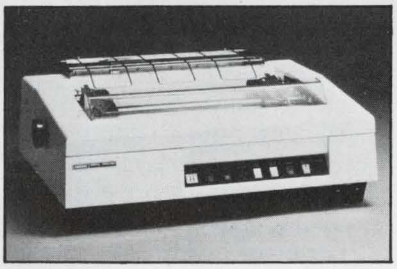

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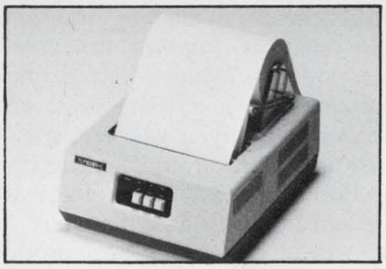

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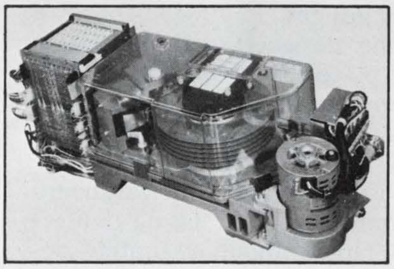

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tacts are deposited. Between the layers is an insulation layer perforated with holes over the contact locations. An overlay with custom graphics covers the top membrane. Pushing the area over a hole causes the upper membrane to move 4-10 milli-inches to momentarily contact the lower layer, which is either flexible or rigid. If rigid, connections are made to it through pins, tabs, pads, connectors or ribbon connectors; if flexible, connections are made through an integral part of the panel, a flexible "tail", upon which are deposited the conductive tracks. If flexible, an adhesive backing permits attachment to a rigid surface, such as the front of an instrument housing. If rigid, fastening is done mechanically.

On the overlay (which is optional, but usually used) attractive symbols, designations and other graphics can be lithographed or screened in up to 15 colors.

Although most membrane switches operate from 5 to 15VDC, they can handle up to 30 VDC in a 1 to 50 mA range with bounce time from 1 to 5ms. Open-switch capacitance is near 100pF. Closed-switch resistance is high, and can range from 20 to 500Ω. However, manufacturers are lowering these resistances in newer designs.

Some designers will first physically place displays, switch panels and the like on a cardboard panel in the same manner that they also place components on a correctly-dimensioned piece of cardboard to simulate a PCB. Using double-sided tape without accurately positioning them gives an idea of area left over. The values of the components, of course, are irrelevant; only dimensions are relevant at the conceptual stage.

Membranes Offer Immunity

Environmentally, membranes are immune to most solvents, soaps and grease. Although many are susceptible to aromatic hydrocarbons, lacquer thinner, corrosives and acid, certain resistive membranes can be obtained to operate in such specific hostile environments, but cost more. Unlike other keyswitches, membranes have a higher tolerance to vibration, shock and humidity. However, if humidity or other matter does enter, membrane performance degrades more rapidly than many other keyswitches.

As for cost, variations are great; and, though low cost switches are available, other factors, such as graphics, can greatly increase this value. Many graphics are done on a custom basis; and, although many designers specify custom graphics, and tooling costs are relatively low, this might add an extra $3k to $4k that must be amortized over your own production run. The more color and the more complexity, the greater the cost of customization. Other cost driven factors include panel complexity versus panel circuitry complexity. Given the lowering LSI costs, it may be more cost-effective to use a more complex switching circuit design and a simpler switch panel. Obviously, making one panel do double or triple duty can save on costs. In fact, this approach lends itself to future upgrading of a unit, or to offering multiple versions of your product, yet cuts down on stocking problems and associated difficulties, such as delivery delays and so on.

For more complex requirements, where a single keypad must operate in six, seven or even a dozen modes, custom graphics won't do. One solution is to use physical grids mounted on a hinge, that turn like the pages of a book. This actuates a mode-selection switch either optically or magnetically. Supermarket terminals use such multimode, flip-sheet grid overlays. This requires little operator intelligence and provides small chance for operator error, yet cuts design and manufacturing costs. As for graphics, this is left to the operator, who can simply attach or remove designations to the flip-sheet grid overlays at will.

Although the main purpose of the overlay is for information and attractiveness, it also adds protection to the graphics, as these polycarbonate and polyester sheets are tough and translucent. Although the graphic overlay can be obtained from another source rather than the keyboard/pad

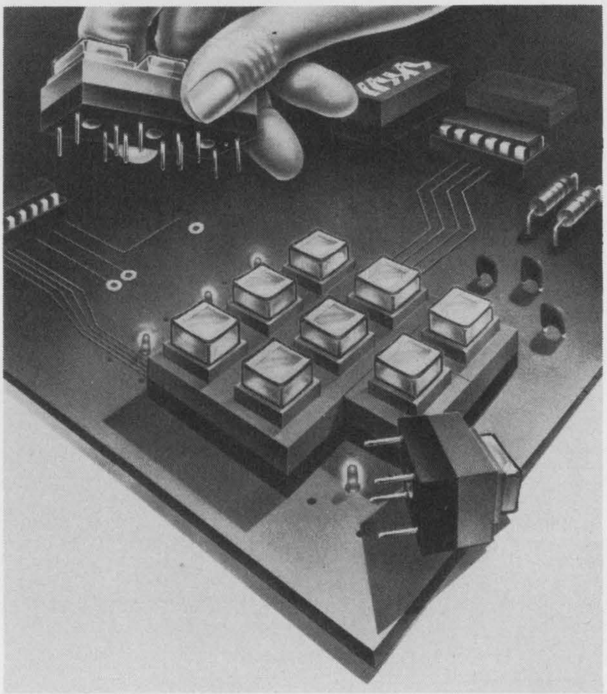

Figure 2: Keyboard modules come in different sizes and in various arrangements that provide for factory-printed or OEM-insertable legends. (Photo courtesy of Grayhill.)

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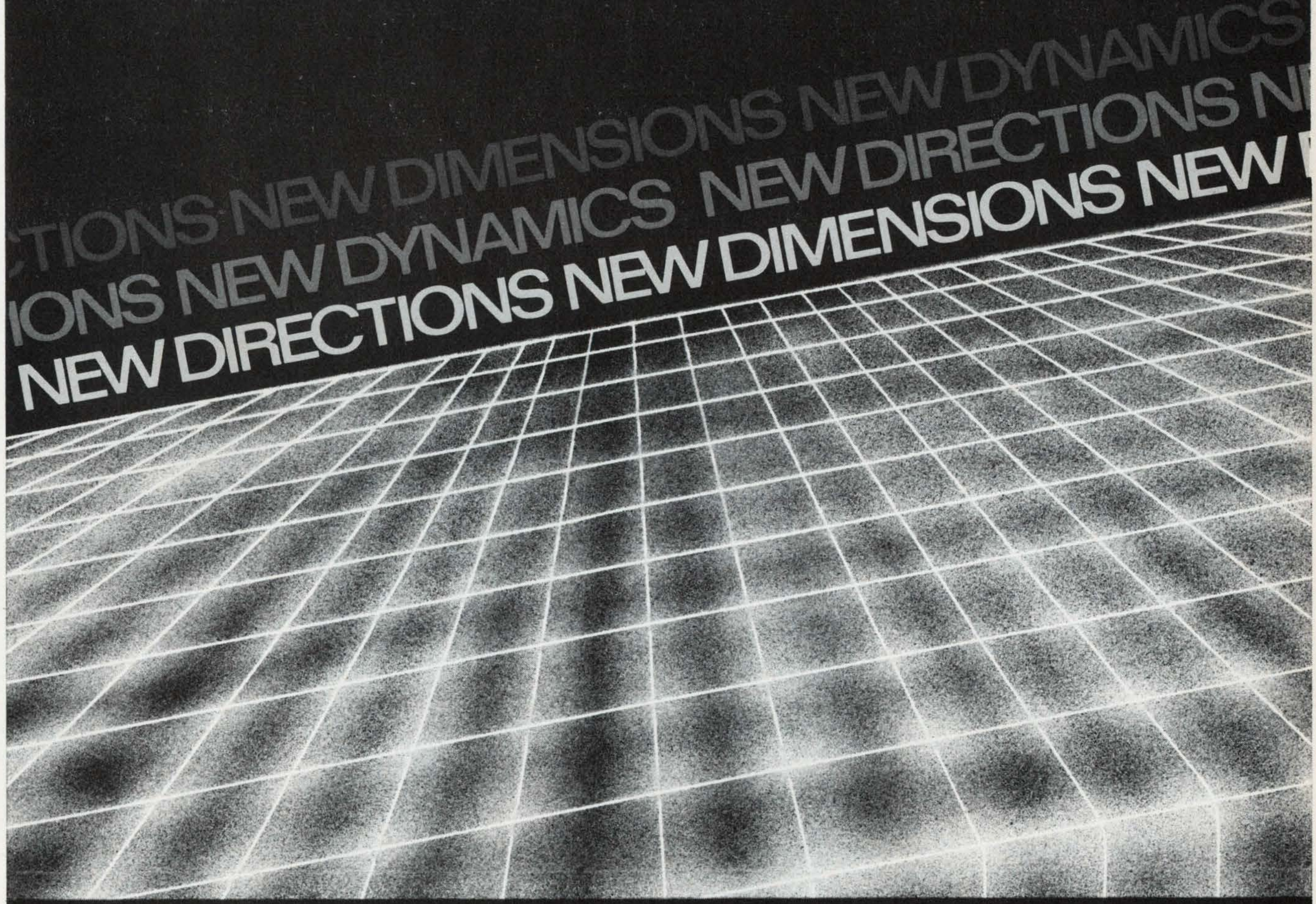
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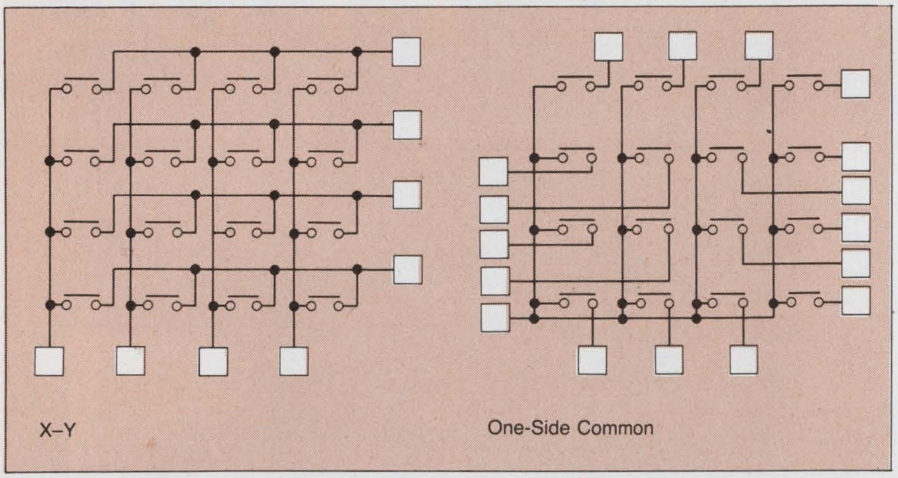

Figure 3: One-side common and X–Y configurations are connection arrangements often found on membrane switches. The one-side common configuration requires many more outgoing connections but provides a discrete output. The X–Y configuration outputs, however, require decoding.

maker (for better graphics), this has its penalties. Mistakes can creep in, and nothing is worse than misregistered graphics, especially if they are off the key holes. Remember that membrane switches are momentary contact, and that to duplicate a single-pole common bus or other key operation requires extra circuitry. Can another, traditional switch do it better at lower cost?

Designers frequently go overboard with membrane switch panels. Examine total costs, not costs in isolation. There is the advantage of low profile (20 milli-inches or so) and simplified mounting, plus sealed construction, but there is also short button travel. This is unsuitable for high data entry uses, because it tires the operators and causes errors. FTM keyboards solve this, and may eventually wipe out other high data entry keyboards.

However, FTMs are still in the early part of their development cycle. Aside from FTMs, tactile feedback and "feel" can produce user uncertainty; and, some users may push buttons twice to be sure.

In layout, the designer must carefully specify active touch area and allow a sufficient border. Specifying a tail length insufficient for proper termination, or one with insulation on only one tail side, can create problems. The tail will be ZIF-terminated, or by friction-fit or insulation-piercing connectors.

In the layout, cluster key contacts to allow termination near the group. Poor layouts use too many switches, are unnecessarily large, and are poorly grouped. Once the vendor finishes prototypes, obviously they must be carefully examined. The earlier testing of existing panels for how well the conductive ink bonded to the flexible surface after several assembly/disassembly cycles, must be repeated for the prototypes. At this stage, the ergonomics people may have some new ideas, and certainly marketing and manufacturing might want some changes.

Static Aggravates Membranes

Static charge can go right through membrane switches, or around and along the insulation, or can be induced transiently through capacitive effects. The small finger contact area of membranes aggravates matters. A thicker overlay helps, as a 10-milli-inch overlay protects at 30kV, and a 15-milli-inch overlay decreases capacitive coupling. Whether this is enough depends on the circuits and layout. Tests may be done in a room simulating the cool, dry worst-case environment. If it fails, then try individual plastic operators and a grounded border to ground static flow. Some panels already possess ground planes to reduce capacitive effects. How-

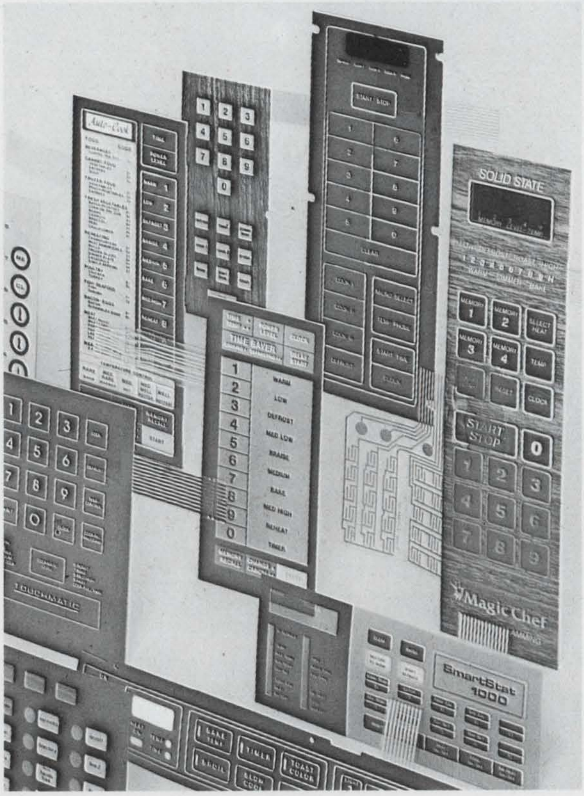

Figure 4: Available in a great variety of standard and custom configurations and designs, micromotion membrane keyboards/pads are available in mechanically-attached or adhesive-backed flexible panels. Both types are thin with an infinite selection in custom graphics and low-cost retooling. (Photo courtesy of Rogers.)

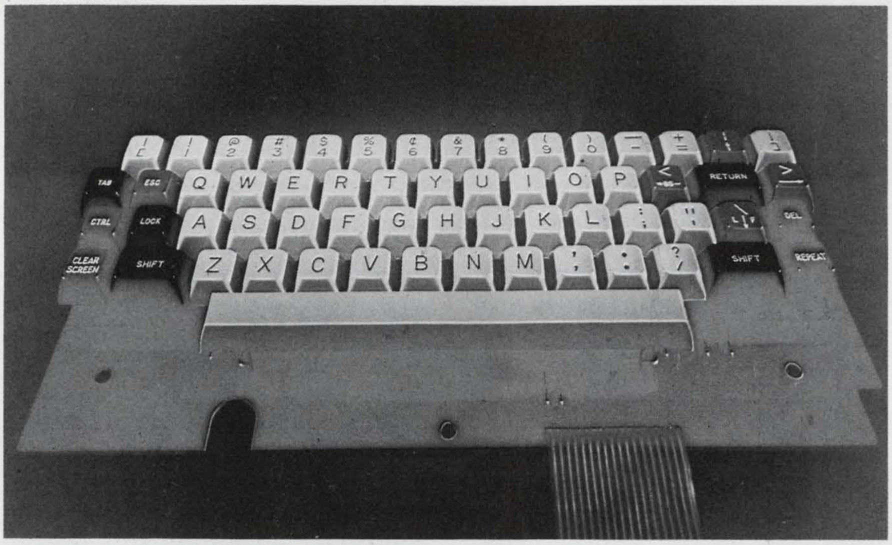

Figure 5: Textured keycaps in a "sculptured" arrangement offer more cosmetic appeal. Different-height caps create a sculptured look to enhance total terminal appeal. Non-glare and multi-color textured caps will not highlight scratches. (Photo courtesy of Stackpole Components.)

ever, borders can increase capacitive coupling.

Contact bounce exists, and can range from 1 to 10 ms. This depends upon how hard the user hits the membrane switch. Better membranes have under 500ms bounce times—times that may not affect many logic circuits. Bounce times can vary with use and aging, and tests in a lab or on a workbench that mechanically cycle keyboards/pads do not simulate actual, intermittent operator use. Most will fail in actual use before the specified rates.

If there is any chance that a slight curvature can occur upon the base, do not use a flexible membrane. Even slight curvatures will reduce contact clearances or close them. In some cases, the use of a rigid panel can be made a part of the enclosure. In either case, the thin structure can permit stacking a couple of parallel PCBs beneath it.

If fingerprints are a problem, then do not use high-gloss polyester overlays: they intensify color, but also intensify smudges. Polyester might do better, but the colors are "softer". For greatest color brilliance, use a polycarbonate overlay. If textured surfaces are needed, vinyl can be used. If nonsight data entry is done, an overlay with embossed keys helps.

As mentioned earlier, membranes operate at about 30V. Some go to 50V. But remember, this will require larger spacings. Do this and some advantages of using membranes are lost. Even momentarily exceeding ratings can weaken membranes. Do not try to handle loads over 1.5 KVA, unless the membranes are specified for it. Also, do not switch inductive loads as this causes arcovers by inductively storing energy that can destroy triacs without snubbers.

Be aware that contact resistance varies: it is 2-10 Ω for rigid; 20-100 Ω for flexible membranes. This is high, but acceptable to logic ICs.

One of the most exciting breakthroughs in data entry is the microproximity sensing switch, such as Tasa's "Ferenstat." These miniature proximity detectors respond to the presence, motion and direction of a human finger. They provide great advantages by eliminating contact noise, resistance and mechanical wear. ☐

NEW
Amkey offers The MPNK-101 Serial or Parallel Keyboard

Amkey's new MPNK-101 Microprocessor based Capacitance keyboard is now available in serial or parallel interface. The MPNK-101 features 1 E-PROM 2758 for encoding and variable baud rates such as 9600, 4800, 2400 and 1200. Other baud rates are available from Amkey with a minor program charge.
The MPNK-101 keyboard is reliable. It has a lower chip count, the silent "no-switch" switch, single +5 VDC supply (±12 VDC RS-232C only) and the N-Key rollover which eliminates the possibility of missing a character during high speed typing.
The MPNK-101 keyboard is versatile. It offers 101 keys including 19 function keys. This keyboard will do word processing, data entry, prototyping, and the same printed circuit board will accommodate both the E-PROM version or the masked version of the microprocessor.
The MPNK-101 keyboard is cost efficient. It has custom designability, lower power requirements and all components are off the shelf.

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Selecting A UPS? Follow These Six Criteria

After the need for a UPS is established, six basic selection areas should be considered.

by Thomas S. O'Neill

Unlike power line conditioners, power distribution centers and motor generators, which address specific aspects of the total power problem, a UPS provides total protection against blackouts, brownouts, line transients and voltage fluctuations. However, specifying the optimum UPS is complex, for there is no standard application—nor, for that matter, a standard UPS.

Nonetheless, once the necessity of UPS protection for a critical load has been established, there are a number of factors that should be considered. Basic selection areas include load requirements, standby battery capability, power distribution and installation considerations, system compatibility, power quality and environmental restrictions.

Load Requirements

At the outset, determine load requirements for the specific application, taking future expansion into account.

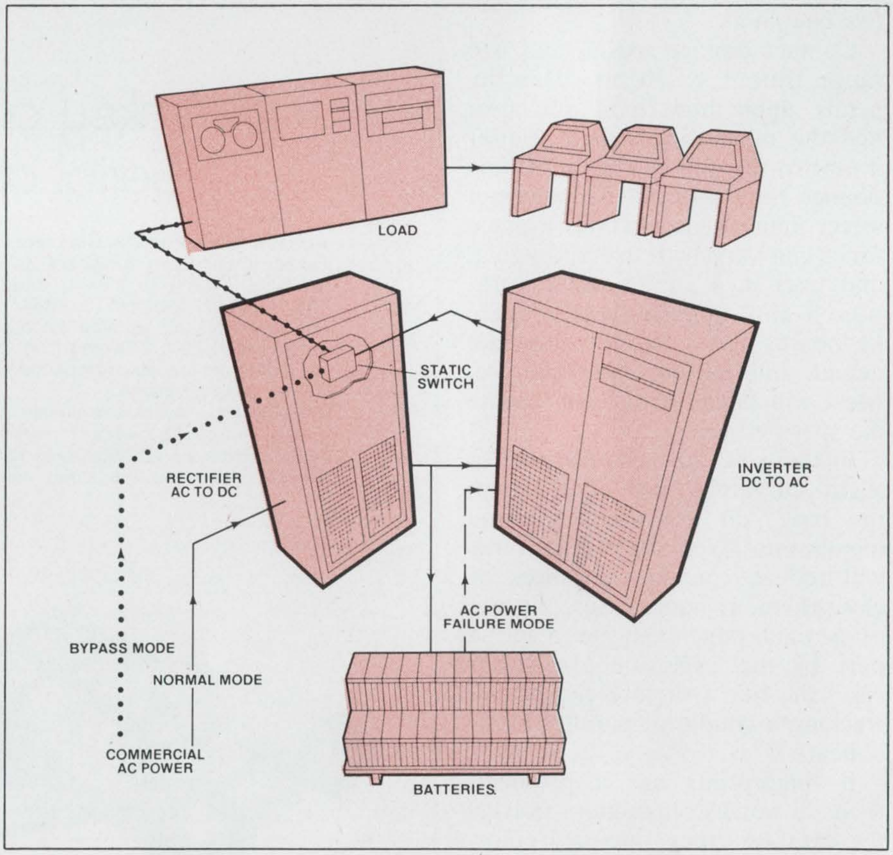
Next, consider secondary systems, such as room lights, alarms, etc., on the basis of priorities and economics. Then, determine specific UPS kW and KVA requirements.

Remember, load requirements will vary considerably, depending on actual load measurements or name plate ratings. The latter typically include significant safety margins that, combined with other allowances, can result in an oversized UPS.

Specific load characteristics are important in applications where the system must handle peak demands on a daily, monthly or annual basis. Five specific load related questions that should be considered are: 1.) Will the critical loads be powered up sequentially? 2.) How severe will unbalanced loading be? 3.) Will the UPS be subjected to leading power factors? Lagging power factors? 4.) What is the overload capability that will be necessary? 5.) Does the load require a no-break transfer to the bypass source in the event of inverter failure, battery failure, or a severe overload?

Standby Battery Capability

After the specific systems that will be powered by the UPS are determined, calculate "reserve time" necessary to support the installa-

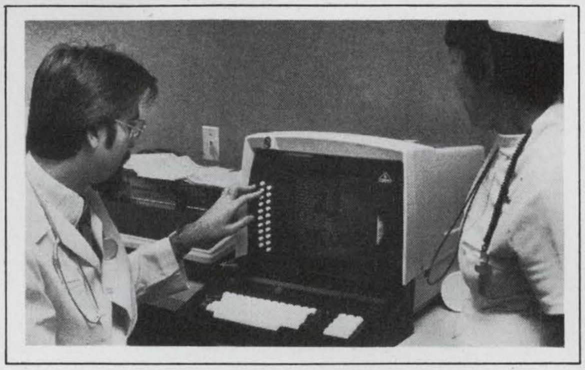


Designed to maintain total continuity of ac power to a critical load, a typical UPS effectively isolates sensitive electrical/electronic equipment from black-outs, brown-outs, line transients, and voltage fluctuations.

Thomas S. O'Neill is Vice President and General Manager of LorTec Power Systems, Inc, N. Ridgeville, OH.

Typical installation where a 125 kW LorTec UPS is powering an Automatic Call Directory (ACD) in an airline's reservations facility.

Specification of the optimum UPS for a particular installation involves a logical process of refinement, designed to determine the specific performance requirements necessitated by the load.



Typical installation where a 30kW LorTec UPS is powering a computerized hospital Patient Information System.

tion—the period for which the inverter can operate using battery power only. Depending upon battery size and load, reserve time is calculated by considering four factors. First, will the battery plant be required to provide prolonged emergency power or just enough to support the critical load until a controlled shutdown can be affected? Second, do location and load requirements necessitate on-site emergency power generation capability? Third, if so, what is the interval between generator start up and the generation of usable power? Although usually only 12 to 15 seconds, this will be unacceptable to many types of loads. Fourth, should the battery be sized to allow time for troubleshooting a balky engine generator or a sticky transfer switch?

Installation Requirements

With the general load requirements and necessary standby battery capability determined, next examine installation considerations. Consider such power distribution factors as utility or power input capacity and mechanics of locating the UPS between the distribution system and critical load. In addition, consider floor space, floor loading, ventilation and cooling.

System Compatibility

To introduce a UPS into an existing installation, be sure it has proven compatibility with the various systems presently operating within the facility. In addition to interfacing with existing or planned batteries, chargers, power sources and alarm systems, be sure the UPS will not interfere with sensitive electronic devices processing and monitoring non-UPS related functions. And, will the UPS comply with EMI FCC regulations? Does the load? Will the installation be properly grounded per the recommendations of NEC and IEEE stds. 142-1972 and 446-1980?

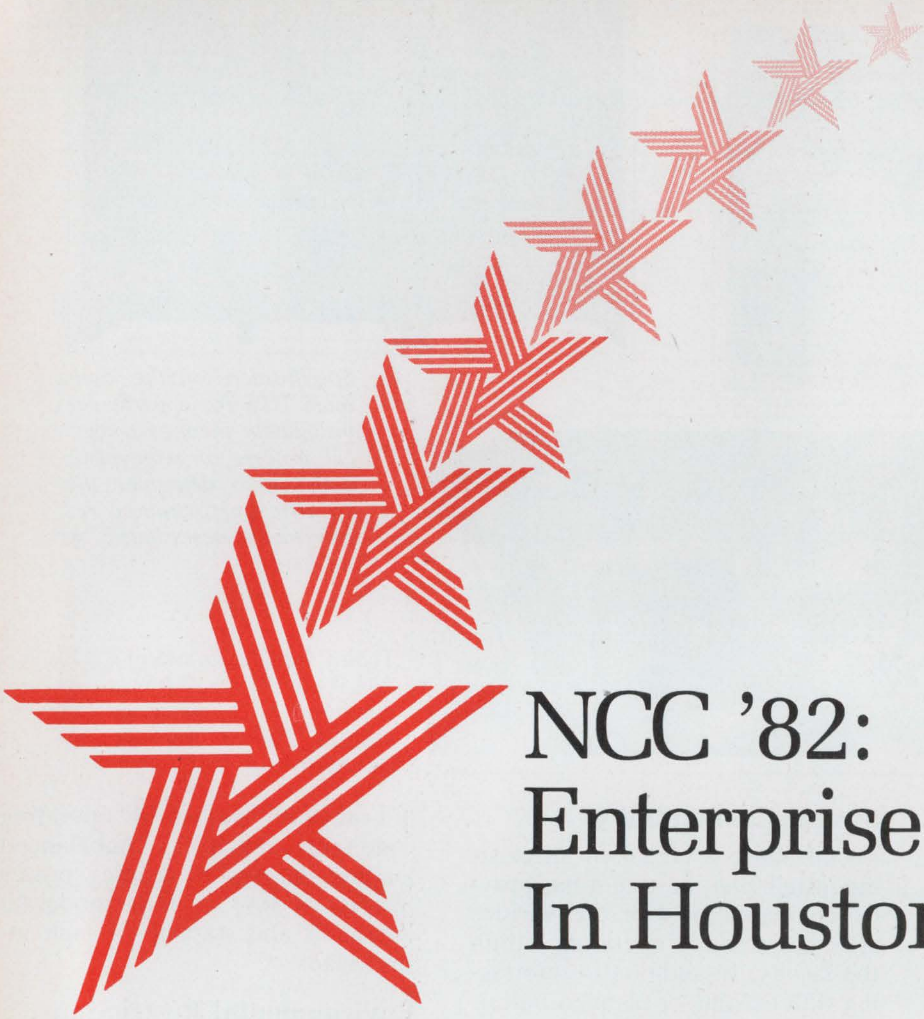
Power Quality

An often overlooked consideration involves the power quality required by the load. Most loads are designed to be compatible with the voltage limits of ANSI Standard ×4.11-1973, which are +5.833% to –13.333%. Exceptionally critical loads may require ± 5% regulation. Some UPS designs can provide much better regulation than necessary under nominal textbook conditions. But, it is far more important to specify a UPS which provides adequate power over a full range of "real world" operating conditions, such as unbalanced loading, lagging or leading power factors as low as 0.8, moderate overloads and start-up of high inrush loads.

Environmental Restrictions

Finally, consider the environmental restrictions that impact UPS performance. Where is the system to be located? What are the ambient conditions to which the UPS will be exposed? What are the ambient conditions to which the battery plant will be exposed? Will the temperature in the power room ever rise above 30°C? 40°C? Will this necessitate the provision for additional cooling capability? How will this impact the reliability and overall efficiency of the UPS operation? What other environmental factors, affecting such things as system reliability, should also be considered?

Once assembled, compare this information to specific UPS systems available. Such a comparison, coupled with an analysis of the system maintenance requirements of the various units and the support services provided by the UPS manufacturer, will enable you to select the optimum system for your application. ☐



NCC '82: Enterprise Takes Off In Houston

Both the small steps and the giant leaps in computer technology that have been made this year will be revealed at NCC.

by David Wilson

To a marketing manager, it's Paradise; to an attendee, it might more closely resemble Purgatory—or perhaps Manhattan during the Friday rush hour. All of these might be appropriate ways to describe the activity expected at this year's National Computer Conference, to be held between the 7th and the 10th of June in Houston.

Keeping the attendees in the midst of all this activity is the first order of business for NCC officials. To dissuade the participants from resting their tired feet in the waters of Galveston Bay, the organizers have provided continuously running films and video tape productions in two theaters at the conference. These include a film from NASA on space research and health, and a Polaroid picture entitled "Graphic Harmony." "We hope all those attending NCC'82 will take time to relax in our theaters," says Eddie Truncellito, the NCC Film Forum Chairman.

NCC'82 will feature exhibits in both the Astrohall and Astroarena by more than 650 leaders in the industry. The theme this year is Professionalism; some of the highlights of the program will include a state-of-the-art review in each of the show's major program areas. Among these, Professor James Emery of the University of Pennsylvania will discuss the management and economics of information systems, and Mr. Robert Frankston, Software Arts, will review Personal Computing.

It is the intention of our preview to highlight specific areas of interest that the attendee might like to investigate more thoroughly, as well as providing information for those who won't be experiencing

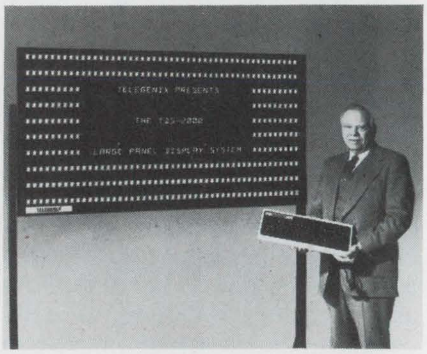


Figure 1: Telegenix's TD2000 display is remote controlled and may be operated long distance via telephone lines.

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Displays Debut

As always at shows, some developments will be easier to spot than others. In the case of the new Telegenix display screen (**Figure 1**), attendees should have no problem. "Our ten-foot flat panel device may seem a little awesome at first," says John W. Taylor, Telegenix President and CEO, "but its simply an extension of our traditional business." Telegenix's customers in the communications/transportation industries had asked the company to address the need for wide-area, bright light computer displays. "So we developed the series TDS2000", explains Taylor. The huge displays are remote controlled and may be operated long distance via telephone lines.

Still on the theme of displays, but not quite so large, Intelligent Systems will be showing its color graphics terminals and desktop computers. Gary Griffin, of ISC's engineering department, shared with us some of the ideas behind the 8364I, a dot-addressable color graphics micro with 480 × 384 resolution.

"Our color palette allows the user to change a given color to any other color without writing to memory (**Figure 2**). Prior to this addition, changing colors meant changing the status of one or more of the three color guns in the unit—red, blue, and green. The disadvantage was that a change in one color often resulted in undesirable changes in other colors. For example, changing green to black was accomplished by turning off the green gun. But cyan (which is green with blue) turned blue, and white (which is all three guns on) turned magenta."

The company's new color palette technique solves this problem. Memory contains an index of codes, any of which can be assigned to any color. Color changes are made by changing codes assigned to the color. For example, green can be changed to black by changing its code from 02 (green) to 00 (black). But cyan and white will remain unchanged because their codes (06 and 07 respectively) have not been altered.

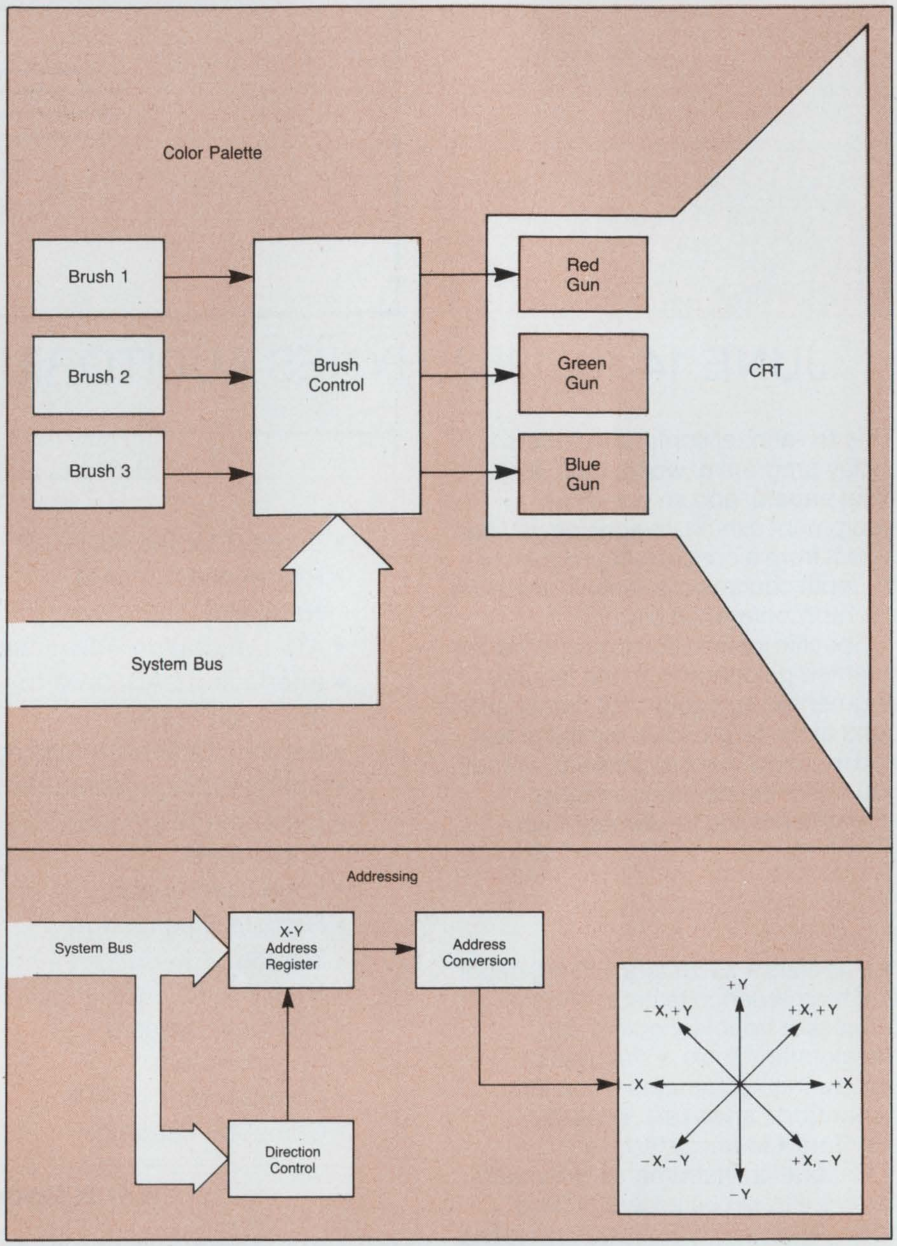


Figure 2: Intelligent Systems' color graphics display incorporates a color palette that allows the user to change a given color without writing to memory.

μP-Based Printers

Although dot matrix printers offer higher plot speeds and reliability than other methods, they traditionally have required time-consuming plot data generation by the host processor, limiting their usefulness in multi-user applications and with systems lacking the necessary software. When custom protocols or special functions are required, additional interface hardware is necessary between the printer and the host processor.

Many of these type of problems can be alleviated by the use of μPs. Chores typically requiring extensive hardwired logic, additional hardware, or substantial user and/or host processor interface, can be downloaded to a μP-based printer system. To realize the greatest potential from this type of printer, it should also be able to accommodate changes in protocol and functional requirements, as well. Trilog has developed its new μP-based

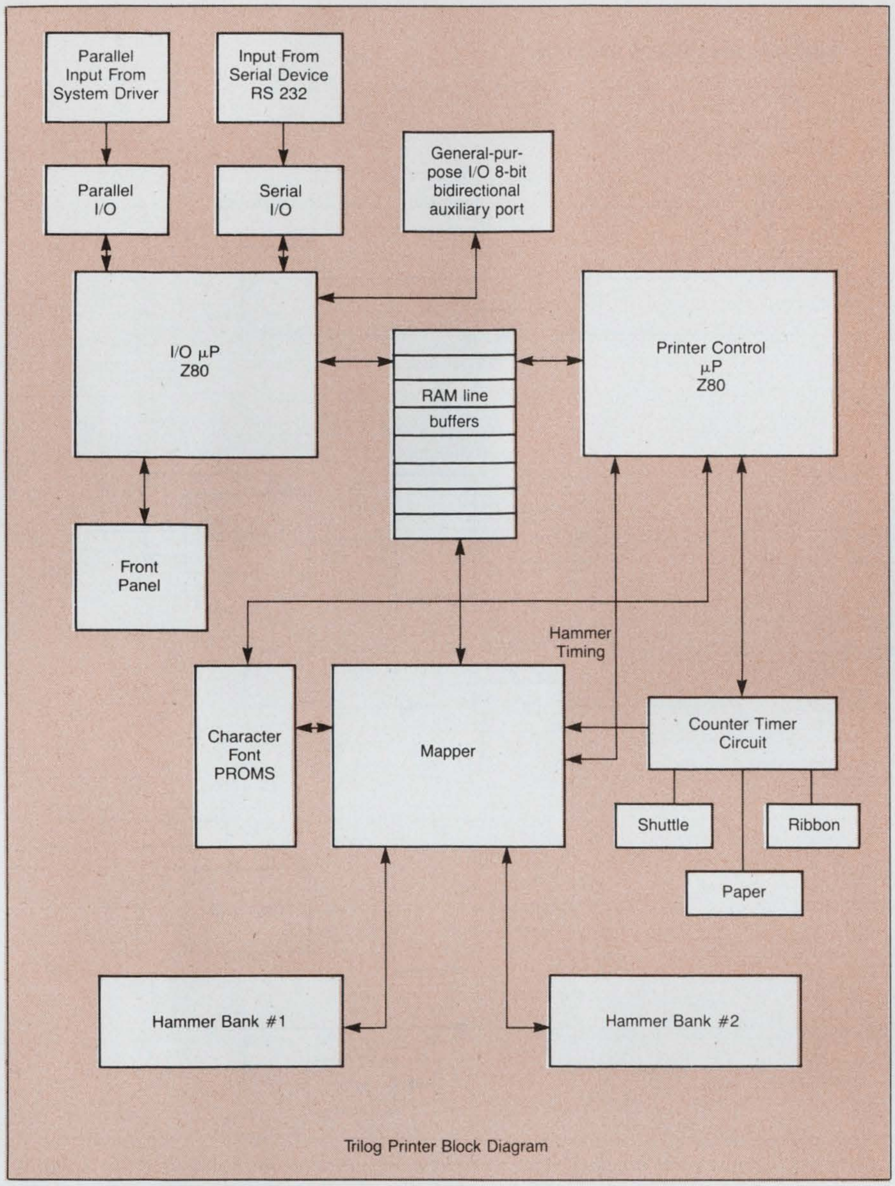


Figure 3: Trilog's dot matrix printer incorporates two Z80s allowing the I/O processor to be changed without affecting standard printer control operations.

distributed-matrix impact printer/plotter, to be introduced at NCC, with this kind of flexibility in mind.

The Trilog system (**Figure 3**) performs two primary functions: it offloads from the host processor the conversion of command data to plot data and/or character code data, and it sets up and supervises all subsequent printing mechanism functions. To increase the functional expandability of the system, these chores are divided between two μPs. Changes can be made to the I/O processor without affecting standard printer control operations.

Primary components in the system include two Z80 μPs, a 2K-byte common RAM buffer, an 8K-byte character font PROM (with capacity for downloading to the printer two 96-character sets), a counter timer circuit and a hardwired mapper.

In standard operations, the I/O processor uses 2K bytes of RAM and up to 16K bytes of PROM to receive and format commands in all standard protocols. Input can be via either RS232C or parallel interface. The resulting plot or character code data is loaded into the 2K byte common RAM buffer, where it is accessible by the printer control μP. This μP then sets up and monitors a hardwired mapper, which draws on the contents of the RAM line buffer and the 16K-byte character font PROM, generating all dot information necessary to operate the printing mechanism. Timing sequences for shuttle motion, paper drive and ribbon servo are generated by a counter timer circuit designed specifically for use with the Z80 μP.

In the case of special user function needs or a custom protocol, the I/O μP can be reprogrammed to accept and format the new input without affecting overall printer control operations. All operative instructions continue to be received by the printer control processor in the same formatted manner. The printer is also equipped with a general-purpose 8-bit bidirectional I/O auxiliary port, to further expand capabilities. For instance, external disk memory containing forms, formats or other information can be accessed through the port.

In the March issue of *Digital Design*, Bob Hirshon, Managing Editor, discussed the designer's problem of civilizing printers to reduce noise levels in office environments. Taking up the challenge, Anadex will demonstrate a receive only printer (DP-9620A) that features acoustic noise levels below 55dBa, achieved by the redesign of the printer case, and special sound-dampening foam. A sound deflector employed at the paper exit also contributes to the noise reduction.

The DP-9620A is a standalone printer capable of both alphanumerics and graphics. Alphanumeric printing speeds range from 200 characters/sec (cps) to 10 character/in (cpi) for a 7 × 9 dot matrix to 100 cps for a 13 × 9 dot matrix that produces enhanced, "draft correspondence quality" characters. Other character densities are 12 cpi, 15 cpi, and 16.4 cpi. The character repertoire includes the 96-character ASCII set with lower case descenders. For graphics, the horizontal and vertical resolutions are both 72 dots/in.

One to six-part paper with interleaved carbon sheets can be accom-

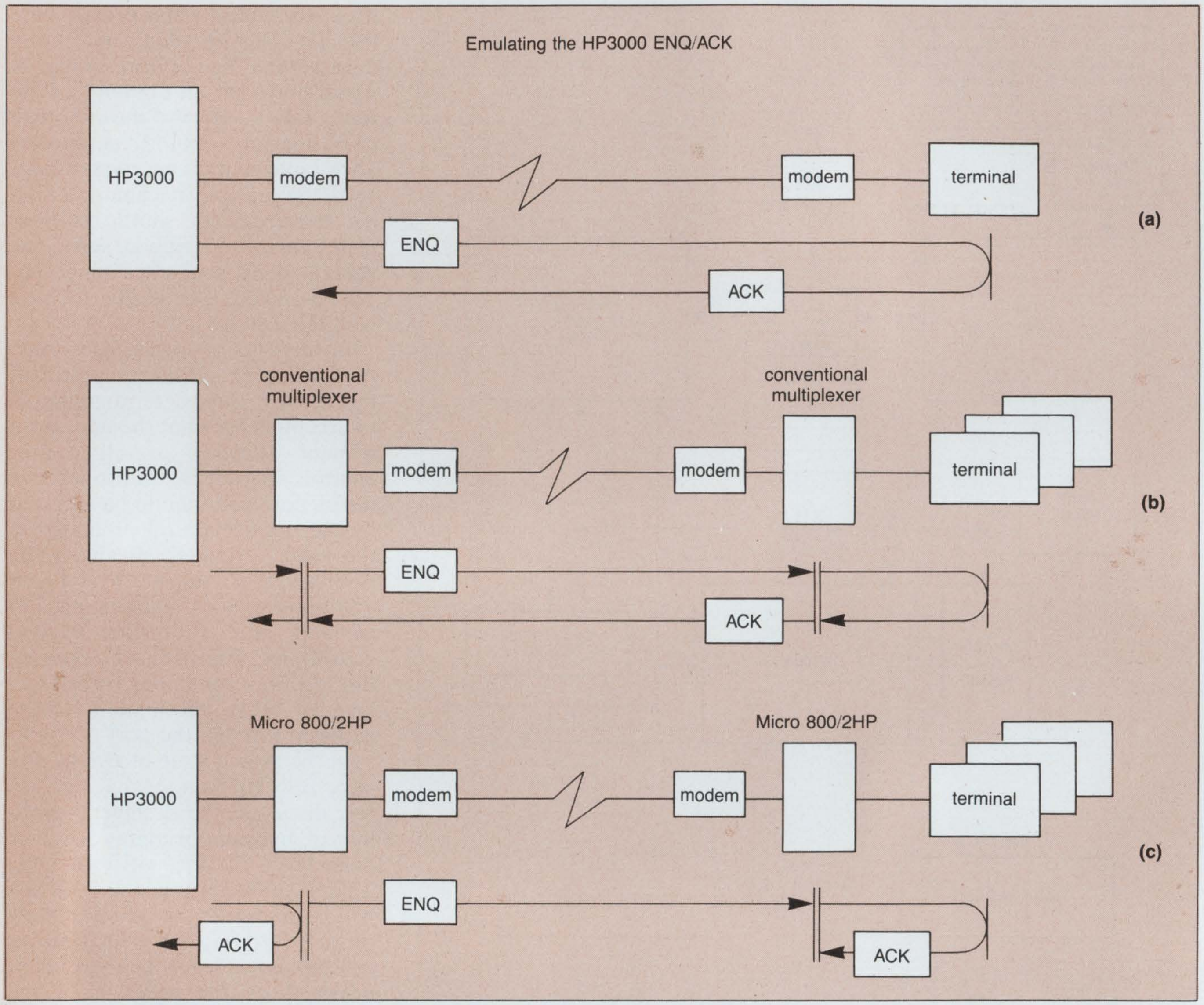


Figure 4a: In the absence of multiplexing, the HP3000 follows each block of data with an ENQ to determine whether the terminal is ready to receive more data. When ready, the terminal responds with an ACK and the host resumes transmitting. Figure 4b: When conventional multiplexers are inserted into the loop, the host's ENQ inquiry is subject to additional delay at each multiplexer while the block of data preceeding it is processed. This can reduce throughput dramatically. Figure 4c: Micom's Micro800/2HP eliminates the extra delay by emulating the ENQ/ACK protocol. When the computer site concentrator receives the ENQ poll from the host, it immediately emulates the remote terminal by responding with its own ACK (and passes the ENQ along to the terminal). The host can begin sending data immediately. The data will be buffered in the remote site concentrator until the terminal issues an ACK. When it does, the remote site concentrator forwards the data to the terminal (but does not forward the ACK to the host).

modated. Form feed is by means of adjustable-width tractors; maximum form width when the paper is centered in the print field is approximately 15-in. Operation is bidirectional logic-seeking.

Two standard interfaces are provided: Centronics bit-parallel and serial EIA RS-232C. As an option, a serial TTY interface is available. Eight serial communications protocols are provided, including three X-ON/X-OFF, four STX/ETX, and ETX/ACK. The DP-9000A and DP-9500A are new versions of the DP-9000 and DP-9500 printers. Front access DIP switches control form length, line width default, alternate characters, skip-over perforation, line spacing, font selection and serial protocols.

Both the CP-9000A and the DP-9500A series provide graphics capability, as well as the 96-character ASCII set. Resolution for the DP-9000A in the graphics mode is 72 dots/in. vertically and 60 dots/in. horizontally. For the DP-9001A it is 72 dots/in. vertically and 75 dots/in. horizontally. Resolution for the DP-9500A is the same as the DP-9001A.

Communications

If the reader did not attend Interface '82 and is involved with the

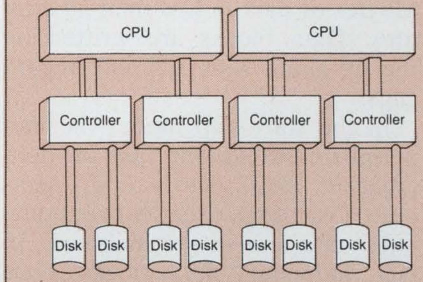


Figure 5a: Typical set up allows the user to talk to disks only through the controller to which they have been assigned.

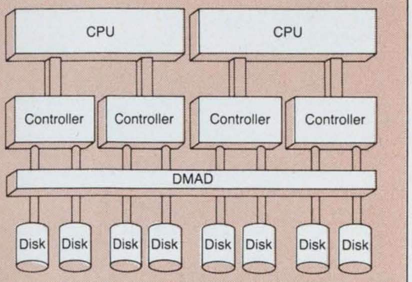


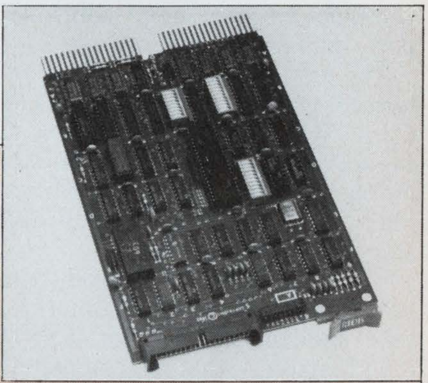
Figure 5b: DMAD allows the user to talk to any disc through any available controller (not just the one to which it was assigned).

problem of providing statistical multiplexing for HP's series 3000 computers, he may do well to visit the Micom stand.

Among the entire product line on show, Micom will introduce a specialized data concentrator (**Figure 4**). Emulating HP's block mode protocol, the Micro800/2HP supports up to eight terminals on a single telephone line. The terminals may operate in either full-duplex or half-duplex mode at data rates up to 9600 bps. The concentrators composite (output) data rate can be 9600, 1800, or 1200 bps asynchronous, or any synchronous rate within that range. (Concentration factors of 4:1 are common—allowing eight 1200 bps terminals to operate on one 2400 bps communications link).

The Micro800/2HP incorporates Micom's Terminal Activated Channel Test (TACT), which allows a non-technical user to test the concentrator, the communications link, and the remote concentrator from any terminal.

A new company, Western Electronics Technology (Houston, TX) are also in the business of improving system throughput. They will introduce a new dynamic multiple access divide (DMAD) (**Figure 5**) that aims to solve disk system contention and reconfiguration problems in large computer systems in-



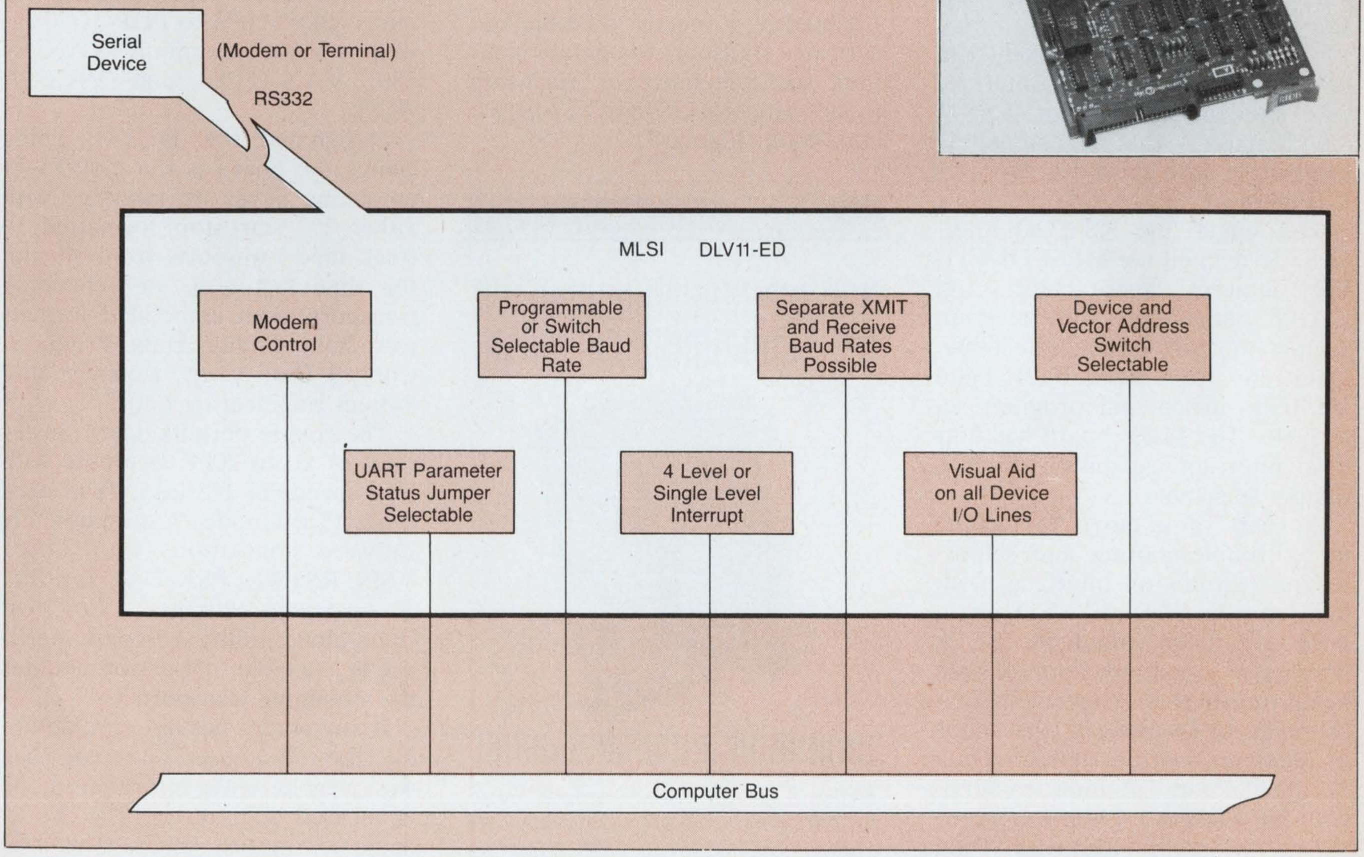

Serial Device
(Modem or Terminal)
RS332
MLSI DLV11-ED
Modem Control
Programmable or Switch Selectable Baud Rate
Separate XMIT and Receive Baud Rates Possible
Device and Vector Address Switch Selectable
UART Parameter Status Jumper Selectable
4 Level or Single Level Interrupt
Visual Aid on all Device I/O Lines
Computer Bus

Figure 6: A new asynchronous signal interface with modem control for LSI-11 based systems from MDB Systems.

cluding multiple mainframe configurations. Subsystem contention has been moved from the controller level to the device level by providing additional control and data paths between the controller and disk storage units. Hence, system disks and standby devices can be shared among multiple systems on a demand basis. The DMAD is hardware and software transparent to the host system, with only a 150ns logic delay.

The DMAD permits up to four peripheral controllers to be attached to each peripheral device access. Scanning at 100MHz, the DMAD provides the requesting controller with an immediate response to a read/write request. The DMAD locks on the requesting controller, and upon completion of the requested function, continues scanning of the next controller port, thus preventing lockout.

The first model is designed to interface up to four Control Data Corp Model 7155 controllers to Model 885 disk storage units. Additional models will be produced later for the other popular disk storage subsystems.

MDB Systems will introduce a new asynchronous serial interface with modem control for LSI-11 based systems that is completely compatible with the DEC DLV11-E (**Figure 6**).

The single line RS-232C interface, designated the MLSI-DLV11-ED, features device addressing, UART parameters and interrupt vectors that are switch selectable. Data rates from 50 to 19.2K baud are both switch and program selectable. The MDB board has four level interrupt capability which is jumper selectable.

As part of a move to include more troubleshooting and self-assessing features on interface modules, the MLSI-DLV11-ED has a series of edge mounted LEDs which give visual indication of data being transmitted or received. Seven other LEDs indicate the status of modem control signals, Data Terminal Ready, Request-to-Send, Carrier Detect, Clear-to-Send, Ring, Secondary Received Data and Secondary Transmitted Data.

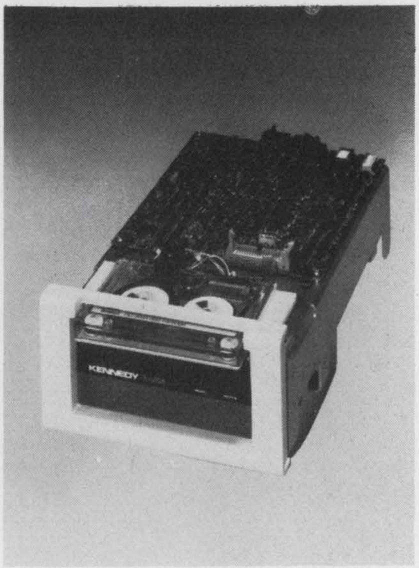


Figure 7: Kennedy's cartridge transport design incorporates a servo-board that removes power should the cartridge jam.

The presence of the LEDs eliminates the need for a breakout box or other device to assess line activity.

Drives To Interfaces

Claimed by Kennedy to be the first cartridge transport to operate in either the streaming or start-stop mode, Model 6455 may be worth a close look (**Figure 7**).

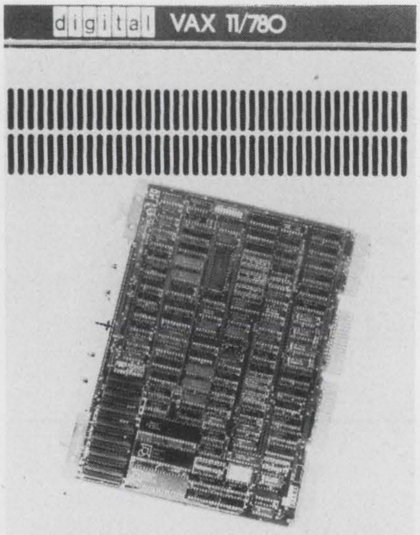


Figure 8: Dilog's new interface board for DEC minis, the DU132 permits data transfer rates of up to 200K bytes per second.

In the streaming mode, the Model 6455 stores or restores 20 Mbytes of data in less than 20 minutes. Data blocks are written on the fly along with 1.2″ interrecord gaps.

In the start-stop mode, the unit permits consolidating files on non-adjacent disk sectors and tracks onto a cartridge using conventional data-management techniques. In fact, individual data blocks, once taped, may be edited or replaced without disturbing other previously written records. Cartridges recorded in the streaming mode may be read in the start-stop mode and vice-versa.

According to Kennedy, Model 6455 exhibits an order-of-magnitude better data reliability than competitive drives; the Model 6455 has a 1×10^{10} soft error rate and a 1×10^{11} hard error rate. MTBF is claimed to be in excess of 5,000 hrs while MTTR is less than 30 minutes.

Still in the field of streaming and start/stop tape backup, Distributed Logic (Dilog) will introduce a new interface board (**Figure 8**) for DEC minis (PDP-11/34 to PDP-11/70) as well as VAX superminis (VAX-11/750, VAX-11/780 and VAX-11/782s).

Designated the DU132, Dilog claims the board is the first TS-11 emulating device to interface with either ½″ start/stop formatted 9-track tape transports from all major manufacturers, or streaming transports with embedded formatters from Cipher Data Products, Control Data Corp, Kennedy and System Engineering Labs.

The couple permits data-transfer rates of up to 200K bytes/sec with tape speeds to 125 ips. When used in start/stop mode, it is completely software compatible with DEC, VMS, RSTS/E, PSX-11M, and RT-11 operating systems. A low-cost stand-alone utility software package is available that accommodates the streaming transports.

If any reader has any trouble filling the ubiquitous shopping bag with new product information, he is advised to stop by the Nissei Sangyo America stand. The US-based OEM sales organization for

Hitachi and Hitachi-affiliated companies will unveil more than a dozen new products, already established in Japan but new to the US market. They include a 16-bit μC system based on Intel's 8086 CPU (with peripheral options that include color graphics and voice synthesis), video display monitors and Winchester disk drives.

A new Multiuser Winchester system that supports up to four terminals and features a 2MHz 6809 CPU, 120 KBytes of static RAM, a 19 MBytes 5¼″ Winchester hard disk, a 1MB (unformatted) 5¼″ floppy and 4 serial I/O ports will be launched by Gimix (Chicago, IL). The system has a unique ability to select between two operating systems, under software control, as well as providing the user with the option of using either the 9511A or 9512 arithmetic processors. The 9511A offers 16 and 32-bit fixed point and 32-bit floating-point arithmetic and a variety of transcendental functions, such as sine, cosine and square root.

The 9512 offers 32 and 64-bit floating and fixed point addition, subtraction, multiplication and division but none of the transcendental functions; the use of these devices can take much of the burden of mathematical calculations off the processor.

The system price of $8998 includes OS-9 level 2, a Unix-like, multi-user multi-tasking operating system and the OS-9 debugger, text editor and assembler. Languages available include Basic 09, Pascal, CIS, Cobol and C. For the money, the buyer also gets a GMXBUG/FLEX monitor/operating system combination, capable of running any software written for FLEX.

Roundup

The reader can be certain that a greater number of new products will be shown in Houston than it was possible to include in this preview.

The editorial team of *Digital Design* will be at the show in force, available at the Morgan-Grampian booth, and awaiting your comments and inputs.

See you at the show! ☐

— ATC ANNOUNCES —

GRAPHICS 810

PLUG-IN CONVERSION BOARDS

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☐ **MODEL 190T** Low-Cost Tektronix™ Push-Button Hardcopy

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Boards also offer 95-character software fonts, barcode and block graphic charactes, programmable expansion, 9,500 character print buffer.

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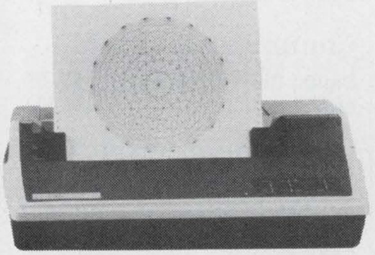

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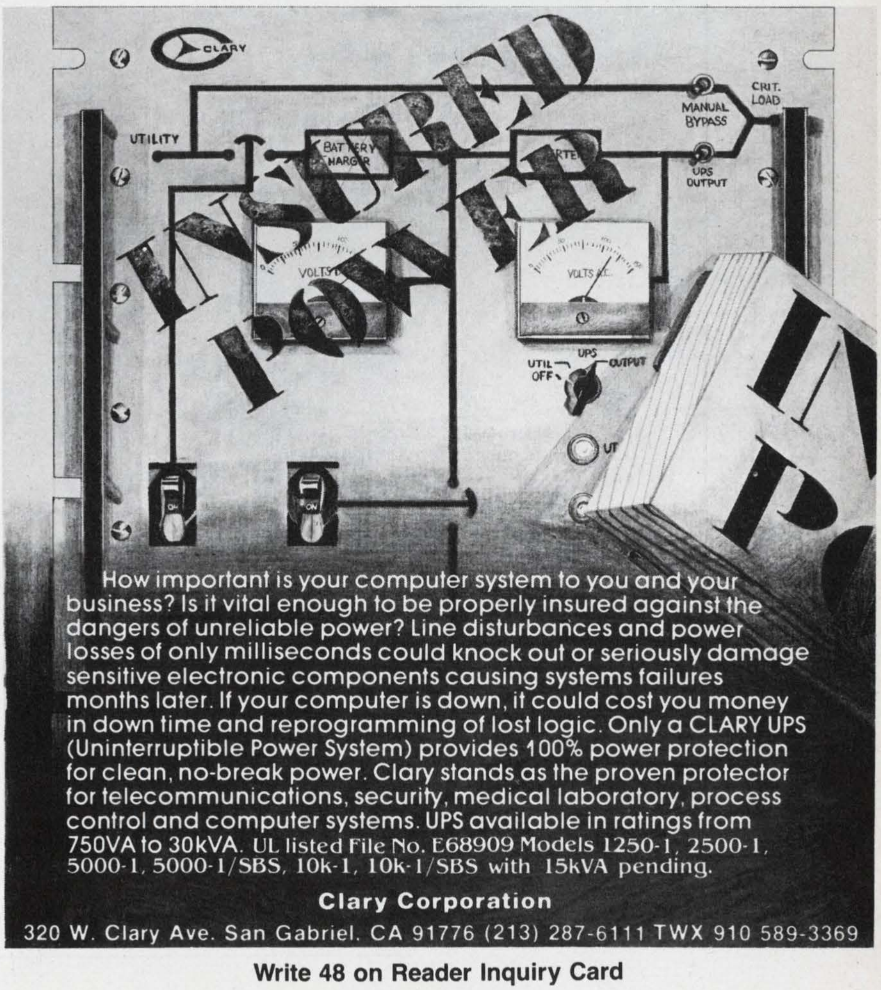

How important is your computer system to you and your business? Is it vital enough to be properly insured against the dangers of unreliable power? Line disturbances and power losses of only milliseconds could knock out or seriously damage sensitive electronic components causing systems failures months later. If your computer is down, it could cost you money in down time and reprogramming of lost logic. Only a CLARY UPS (Uninterruptible Power System) provides 100% power protection for clean, no-break power. Clary stands as the proven protector for telecommunications, security, medical laboratory, process control and computer systems. UPS available in ratings from 750VA to 30kVA. UL listed File No. E68909 Models 1250-1, 2500-1, 5000-1, 5000-1/SBS, 10k-1, 10k-1/SBS with 15kVA pending.

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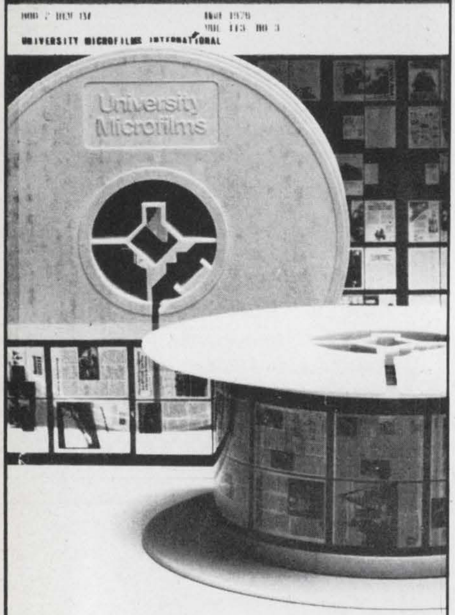

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Product Index

To help you find the products you need, we've compiled a subject index of the ads and new products that appear in this issue. Organized by general product area, the listings include the name of the manufacturer, the page on which the product appears and a write number for additional information on that product. Bold type indicates advertised products.

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This index is provided as an additional service. The publisher assumes no liability for any errors or omissions.

World's First Color Logic Analyzer

Tektronix, Inc. has introduced the world's first color logic analyzer—a color version of its DAS 9100 System.

The DAS 9120 color logic analyzer is a modular digital analysis system housing both data acquisition and pattern generation card modules in the same mainframe. Offered in a variety of data widths and speeds, these modules are combined in the mainframe to match the user's application needs. Data acquisition widths of up to 104 channels and speeds to 660MHz give state-of-the-art performance, and the interactive pattern generator allows simultaneous stimulation and acquisition from a device under test.

The DAS 9120 series represents the first use of a color display in test and measurement instrumentation. Tektronix claims that color significantly enhances the interface between the operator and the logic analyzer and, when compared with other forms of information coding, color can reduce human response errors by 80%. Color may also offer a decided advantage when applied to tasks such as glitch detection and cursor-based measurements of timing information.

Although new to test and measurement, color has a long and successful history in many different types of display environments. Since the human brain is naturally equipped to process color information, color is a logical choice for encoding complex displays, such as those found in logic analyzers.

Three colors—red, yellow and green—were picked for the CRT display, as the spectral spacing between these colors makes them easy to identify and separate with the human eye. Each color has been applied to specific information on the DAS 9120 display.

For quick analysis of displayed data, "background" information, such as line labeling, is separated from "foreground" information, such as timing diagram. Programmable menu fields are color-separated from other fixed fields and menu prompts and cursors are color-coded in red for faster recognition and interpretation.

All acquired state and timing data are displayed in yellow, with supporting background information in green. Items that require focused attention, such as cursors and error messages, are presented in red. Glitches on the acquired data are highlighted in green.

The DAS 9120 also incorporates other features such as "Delta-time" which automatically calculates time intervals between selected sample points. In addition, mnemonic tables are available which support popular μPs and communications formats.

"Delta-time" provides greater speed and accuracy in measuring

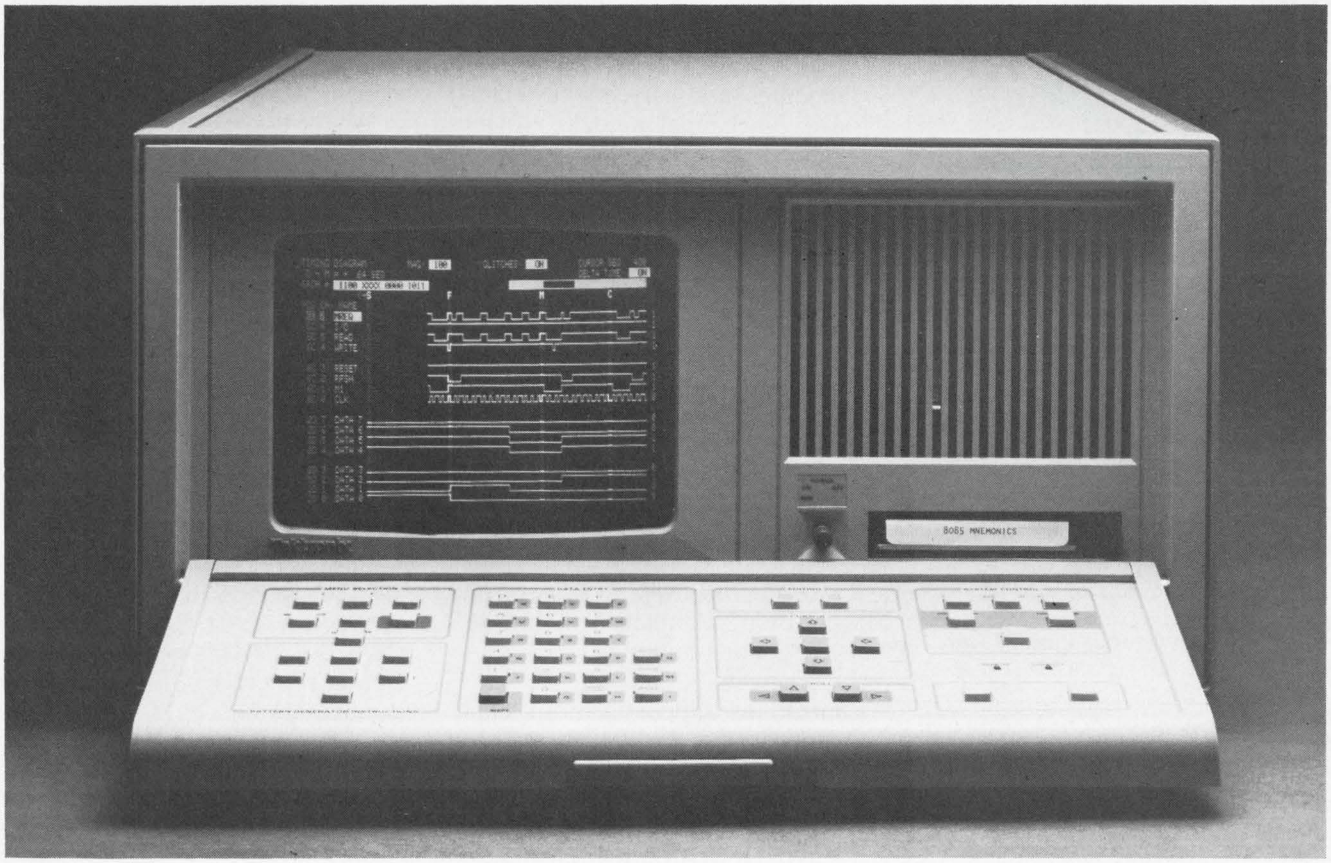

Figure 1: Color is used in the display of this logic analyzer to allow faster interpretation of displayed data.

the time between selected events. After the cursors are positioned at two selected events on the timing diagram, the time difference can be read directly in the "delta-time" display field. The display indicates the appropriate time units, such as milliseconds, microseconds or nanoseconds.

The new mnemonic tables are available on DC-100 tape cartridges for the DAS 9100's optional tape drive and use the system's user-definable mnemonics capability. Mnemonics for the Z80, 1802, 6800, 6802 and 8085 are available as well as communications formats for ASC11, EBCDIC and GPIB.

The DAS 9129 color mainframe is priced at $7850. Modules, priced from $3,500 and selected for their specific data acquisition and pattern generation capabilities, are in the form of cards that plug into the six available slots of the mainframe. Four standard system configurations priced from $15,000 to $30,000 are also available.

For data acquisition, three modules are currently available. The 32-channel module provides 25MHz sampling both synchronously and asynchronously with 512 bits per channel memory and two clock qualifiers. The 8-channel module provides 100MHz sampling both synchronously and asynchronously with 512 bits per channel memory, separate acquisition and glitch memories, and one clock qualifier. The 4-channel module provides 330MHz sampling both synchronously and asynchronously with 2048 bits per channel memory. A high resolution mode is also available which provides 660MHz (1.5 ns resolution) on 2 channels with 4096 bits per channel memory.

These modules can be intermixed to support various applications. Up to 104 channels of data acquisition are available at 25MHz, up to 32 channels at 100MHz, up to 16 channels at 330MHz, and up to 8 channels at 660MHz (1.5 ns resolution).

A trigger arming mode allows high speed data acquisition modules monitoring hardware activity to be triggered from slower speed modules tracking software flow, with acquired data time-aligned in both timing and state table displays.

For pattern generation, a module is provided with 16 data output channels at 25MHz, plus two independent programmable strobes. This can be extended to 48 or 80 channels of pattern generation with up to 10 programmable strobes by adding one or two 32-channel expander modules. The pattern generator also has several external control inputs, including branch on interrupt, that allow interaction with the system under test.

Pattern generation can be used interactively with data acquisition and various test programs can be created using the pattern generator's instruction set, which includes counting, looping, and nested subroutining. These programs can then be used to stimulate the hardware circuitry while the data acquisition cards are used to capture the results.

An optional DC-100 magnetic tape drive allows the user to both load and store all the system's setup information, pattern generator programs and tests, reference memory data and mnemonic tables. The tape can provide for transfer of test and evaluation routines to production test personnel and service organizations.

The optional communications package consists of an RS-232-C port, GPIB interface, and a standard video output. The RS-232-C port and GPIB interface allow complete remote programmability of the DAS 9100 from a host computer or GPIB controller. Two DAS 9100's can also be operated remotely in a master-slave configuration.

The video output enables the user to obtain a hard copy of the contents of the CRT screen for records and documentation with a Tektronix 4612.

Write 198

MICRO-PROCESSOR COMPATIBLE THERMAL PRINTER

Model MAP-20P is a 20 column, alphanumeric panel mount printer that accepts 8 bit TTL parallel data at rates >2000 C.P.S. Complete with μP controlled timing, character generation, printhead-drive, stepping — motor circuits, the unit also has its own self-test program and AC power supply. Weight is 4.2 lbs. and panel space is 14.8 sq. inches. Price is $625.00 and in stock:

Memodyne
CORPORATION
Subsidiary of Computer Products Inc.
220 Reservoir Street
Needham Hgts., MA 02194
617-444-7000 Telex 92-2537

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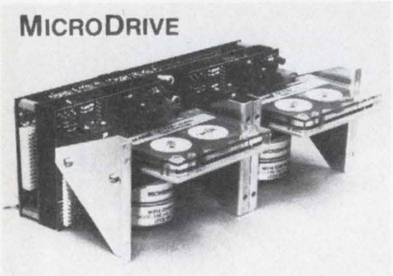

DC100 CARTRIDGE DRIVE HAS SMART I/O

MicroDrive/OEM now features a micro processor based I/O. This unit performs all control and formatting for quick systems integration. A high level command set (22 commands) allows full peripheral status for the model 125I/O. Serial and parallel options are available priced as low as $400 in OEM qty.

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CMOS/SOS SBC Dissipates Less Than 5W

Originally established as a spinoff from the General Electric R & D Center, Mikros Systems is now manufacturing a μP (the MKS16) and a single board computer based around the 16-bit device. On chip functions include 16 general-purpose registers, a full 16-bit arithmetic logic unit, 2 accumulator/shift registers, status register and microinstruction decode logic. All signal inputs and CPU outputs are designed to be either TTL or CMOS compatible.

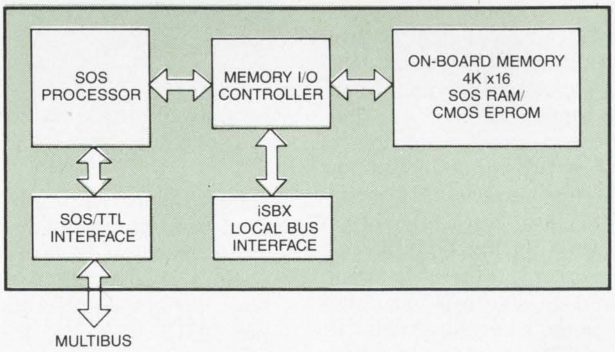

Figure 1: Maximum configuration of Mikros Systems' Multibus-compatible μP.

Surrounding the processor are additional CMOS/SOS logic devices that provide a number of system options. The minimum system consists of 6 chips—one MKS16, one SOS gate array that provides the Multibus Interface, and four SOS control ROMs—and dissipates less than 750mW.

The maximum system **(Figure 1)** adds 4K x 16 of on-board SOS RAM, a local bus interface (iSBX-compatible) and TTL-level drivers for off-board communication, and dissipates less than 1.5W at the maximum operating clock frequency of 5.5 MHz.

Providing back-up, the MKS16 development system contains an SOS/TTL processor board that is plug compatible with the MKS16 all-SOS SBC, two additional Multibus boards providing memory and I/O, and standard off-the-shelf Multibus packaging.

Write 197

Special Issue

1982/83 Computer Compatible Directory/ Technology Review.

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CAD/CAM SYSTEM

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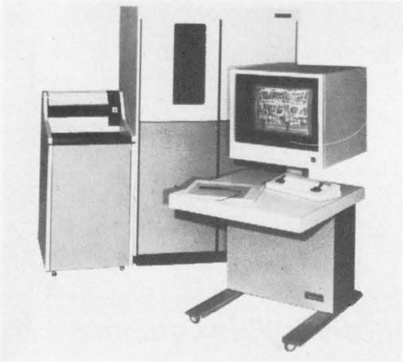
Video Designer includes the hardware and software components needed for either mechanical/architectural or PC board design applications. It is designed for small- and medium-sized engineering organizations, or first time CAD/CAM users requiring a low-cost one or two terminal system. The basic system includes a Central Processing Facility consisting of a PDP-11/34, an Applicon Graphics-32 Display Processor, a 200 MB disk subsystem and an 800/1600 bpi dual-density magnetic tape subsystem. It also features a B&W video graphics workstation and a console alphanumeric terminal. The system supports either 2D or 3D applications software and a maximum of two graphics work-stations. It allows users to add optional hardware and software components and is upgradeable to a multi-terminal system with a choice of plotters and peripherals. The basic Video Designer system is $150,000; a second B&W terminal may be added for $40,000 or color terminals may be substituted for an additional $15,000. **Applicon Inc,** 32 Second Ave, Burlington, MA 01803 **Write 170**



COMPUTER SYSTEM

Fail-Safe Hardware Architecture

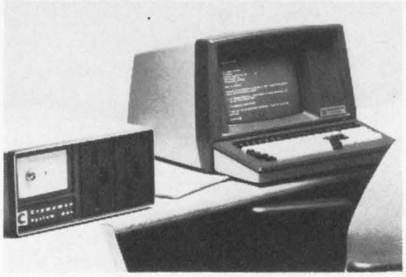
The Failsafe system features an innovative software development system that: automates the logical process of structured programming for developing applications software; reduces the cost of maintaining applications software; and reduces the possibility of downtime caused by software failures. It eliminates common sources of programming errors by automating major portions of the development process and thereby prevents the writing of programs that could cause system failures. Designed for on-line use, powerful individual computers are provided at each of the 32 workstations the system can support. A basic system configuration including two 80MB disks, two 16MB disk cartridges, two data base manager computers, two data base controller computers, two 200 cps printers, one workstation, one supervisor station, dual power supplies, and software is $79,400. **DOSC Inc,** 175 I.U. Willets Rd, Albertson, NY 11507. **Write 172**

Note: The above product from DOSC was inadvertently listed in the February issue with the incorrect photo. For information on the Vector Graphic system that was pictured, see the March 1982 New Products section.

DESKTOP COMPUTER

Multi-User Capability

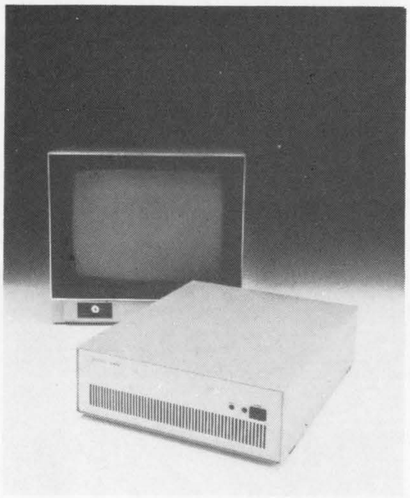
The basic System One is provided with a powerful Z-80A based CPU, 64k of RAM, a printer interface, and dual quad-capacity 5″ floppy disk drives. These disk drives provide 780k of storage capacity. The system is expandable to 256k of RAM and up to three users, and a color graphics subsystem may be added. Also available is the CS-1H which has a 5″ Winchester drive providing 5MB of disk storage. Broad software support with a number of end-user oriented packages is provided. The System One (Model CS-1) is $3995. **Cromemco Inc,** 280 Bernardo Ave, Mountain View, CA 94043. **Write 171**



COLOR GRAPHICS

Display Controller And Graphics Subsystem

The OMEGA 400/DC display controller is designed to interface with most popular minicomputers. The 400/GS is a complete graphics subsystem containing both the 400/DC controller and a 19″ high resolution color monitor. It provides true 1024 × 1024 pixel resolution at the price of today's 512 resolution products. Its single-board electronics and built-in test and diagnostic capabilities make it reliable and highly maintainable. The OMEGA 400 draws vectors and characters at the high speed of 1 million pixels/sec. Rectangular areas can be filled or cleared at up to 16 million pixels/sec. The screen can therefore be completely redrawn in less than one second. Other features include: four memory planes to display up to 16 colors from a palette of 256 colors; integer zoom; hardware vernier pan; extensive instruction set; and PIXBLT block transfer capability which allows any rectangular area to be quickly moved to or replicated in any location in the display. The 400/DC is $12,900; the 400/GS is $18,100; qty discounts avail. **Metheus Corp,** PO Box 1049, Hillsboro, OR 97123.
Write 178



COMPUTER SYSTEM

With The Power And Versatility of UNIX

Employing the UNIX Version 7 operating system, and configured around the Motorola MC68000 μP, the System 83/ is also fully IEEE-696/S-100 compatible. By utilizing the 68000 running at 8 MHz, it can execute ap-

proximately one million instructions per second. The CPU provides 16-bit data paths and a 32-bit internal architecture. However, the System 83/ has the capability of supporting up to 16MB of directly addressable memory. Using Dual Systems memory boards, up to 4MB can be resident in the enclosure. The UNIX Version 7, ported by UniSoft of Berkeley, Calif., includes many of the Berkeley enhancements such as C-shell and the Visual Editor, as well as the "C" compiler, a 68000 assembler and a linker/loader. The recently announced Western Electric System III UNIX will be ported to the System 83/ during the first half of 1982. System/83 versions range from floppy-disk based systems at $8295 to the multi-user/multi-tasking System 83/40 with DMA controller and 40MB of memory on a single Winchester disk at $23,950. **Dual Systems Control Corp,** 720 Channing Way, Berkeley, CA 94710. **Write 173**

OEM GRAPHICS SYSTEM

For CAD, Simulation And Other Scientific Graphics Applications

The G-6150 color/monochrome graphics system incorporates the G-6000 Advanced Display Computer, a state-of-the-art graphics processor, refresh memory and a post processor. The 16-bit processor is a PLA oriented, bit slice design with internal instruction execution times as low as 160 ns. It is equipped with 16kB of PROM and 112kB of RAM. Also included in the system is a refresh memory of 768×512×4 full bit map, 60 Hz non-interlaced for flicker-free viewing. Sixteen colors or monochrome shades can be chosen from a palette of 64. Selectable raster DMA from the host to the refresh accommodates the requirements of imaging. An Animation Assist Mode wherein the graphic is automatically erased during the read refresh cycle reduces by 50% the time to erase and rewrite a graphic in a new position. A number of options are available for the G-6150 to allow expanded capability in OEM systems. Under $13,000. A dual channel version is under $17,000 in OEM qty. **Genisco Computers Corp.,** 3545 Cadillac Ave, Costa Mesa CA 92626. **Write 176**

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BUSINESS COMPUTERS

Modern Ergonomic Styling

The 8 bit µP-based systems include 8085 CPU, 64K RAM, serial printer port, parallel printer port, and EIA RS232C port. Special features include choice of 12 or 15″ non-glare CRT in a variety of phosphors. The display rotates 90 degrees and tilts 22 degrees. The detachable, low profile keyboard has 97 keys with special word processing, user function, and numeric keypad areas. Choice of 5¼″ or 8″ dual floppies, single or double sided. Winchester hard disk is also available with floppy back-up. Systems are shipped with CP/M operating system. From $3995 for the SCS510, with dual, double density, 5¼″ floppies, 12″ terminal, keyboard and operating system. The SCS810, with dual, 8″ floppies, 12″ terminal, keyboard and operating system is $4995. **SCS International,** 2635 Croddy Way, Santa Ana, CA 92704. **Write 180**

WORD PROCESSORS

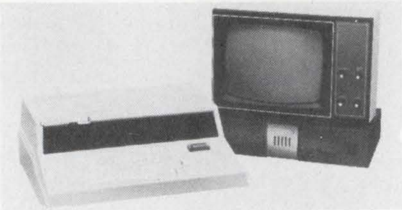
Multi-Function Systems

The VT 201 (single-diskette) and VT 202 (dual diskette) word processors incorporate the most heavily utilized functions of the VT 1000 series. They can be enhanced with the following options: dual sided disk drives, communications, math package, shared printers, alternate character set, dual tray sheet feeder with envelope feeder, Records Management System (RMS), twin-track printer, wide-track printer and TypeReader 3. They are comprised of two trim desktop units. The editor houses the electronic keyboard, single or dual mini-floppy diskette drives and the display screen. The printer unit houses the printer and its power supply. Up to 6 editors may share one printer. The VT 201 is $7505; the VT 202 is $8755. Lease rates are also available. **Raytheon Data Systems Co,** 1415 Boston-Providence Tpke, Norwood, MA 02062. **Write 179**

µC DEVELOPMENT SYSTEM

Also Functions As An Industrial Control System

The DIS-1 system combines in one enclosure a 6502-based AIM 65 with full keyboard, printer and display, 64K dynamic memory, CRT and floppy disk controller modules, a PROM programmer and power supply, plus two double-density floppy disk drives and a 12″ CRT monitor. All required software, including Basic and Forth language is included in the integrated hardware/software system. With the Dynatem disk operating system, the PROM programmer and the various language options, the DIS-1 is a complete development system for software or actual hardware for a planned product. As an industrial microcomputer system, it can be customized for specific applications with any of hundreds of off-the-shelf modules. $4950. **Dynatem Inc,** 20881 Paseo Olma, El Toro, CA 92630. **Write 175**

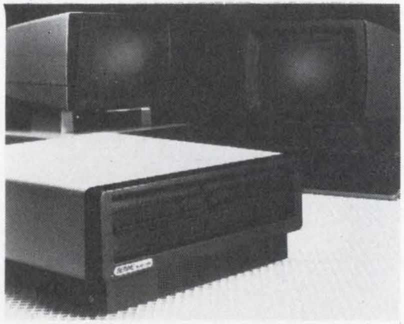


PERIPHERALS

FLOPPY DISK SUBSYSTEM

Double-Sided, Double-Density Floppy For HP Systems

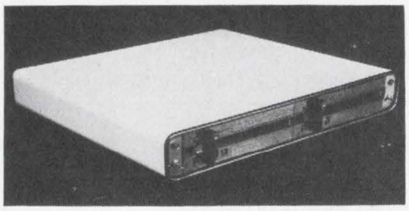
The 2895 subsystem is hardware, software and media compatible with the HP 9895A. It connects to the GPIB, adding 2.36MB of immediate storage capacity to most HP mini, desktop, and personal computers. Storage capacity may be expanded to 4.72MB with addition of a dual-drive slave unit. In addition to reading and writing all HP double-density formats, the 2895 reads and writes the full range of IBM single and double density flexible disk formats. This facilitates the exchange of data programs with other mini and microcomputer systems. $4660, OEM and ISO discounts avail. **Bering Industries,** 747 E. Brokaw Rd, San Jose, CA 95112. **Write 146**



DISK DRIVE SUBSYSTEMS

Twice The Storage In Half The Space

The CMS 1600 disk drive subsystems utilize the new Tandon Thinline DS/DD 8″ drives. Storage capacity for 2-drive units is 2.4 MB and 4.8 MB for the 4-drive unit. The drives are one-half the thickness of standard drives, so two drives can be housed in a standard single-drive cabinet, while four drives fit into a standard 2-drive cabinet. Available in vertical or horizontal 2-drive and vertical 4-drive configurations. The 2-drive units feature optional write-protect switches and LED's. All models include power supply, cables and utilize the standard Shugart-compatible interface for 8″ CP/M disks. $1695 for the 2-drive horizontal or vertical subsystems, $1750 for the 2-drive low-profile unit and $2995 for the 4-drive unit. Qty discounts avail. **Columbia microSystems Inc,** 905 E. Broadway, Columbia, MO 65201. **Write 147**



ERGONOMIC TERMINAL

Multi-Page Display

Designed as an integral part of the NonStop transaction processing systems, and built to meet international ergonomic rquirements, the 6530 terminal has a 15″ diagonal, non-glare screen with green phosphor characters. The 25 line by 80 column screen tilts and swivels to conform to the viewing needs of individual users. The detached, low profile keyboard has a palm rest and two-position tilt adjustment for operator comfort. Up to 8 pages of memory are stored in block mode for high data throughput, or 300 lines in conversational mode

for easy access to previous screen display. It currently accommodates 7 languages with keyboards to match. The 6530 can operate in many combinations of sync or async modes, in half or full duplex, and supports both RS-232C and current loop interfaces. The terminals may be run point-to-point or multipoint. Also provided is an extensive range of editing functions and user selectable video and data attributes. $3200. **Tandem Computers Inc,** 19333 Vallco Pkwy, Cupertino, CA 95014. **Write 151**

IN-CIRCUIT EMULATION

Support Package For The NSC800

This package provides all hardware and software necessary for the ECL-3211 line of universal development systems to perform full-speed, real-time, in-circuit emulation, simulation and software development for the NSC800. Included are the target interface pod, chip driver software and disassembler, macro cross-assembler, linker and universal PROM programmer utility. All features and operating modes of the NSC800 are implemented at all clock rates up to the full rated speed of the chip (4 MHz at 5 V) including the "power save" function which permits stopping CPU operation while maintaining the system clock. Used with the PDP-11-based ECL-3211 development system, the NSC 800 controller provides a 511-record, 48-channel real-time trace analyzer selectively controlled by hardware breakpoint actions or the operator keyboard. The trace analyzer displays data, disassembled mnemonics, status of eight external lines plus all chip status and control lines in a smooth-scroll screen display. $1500. **Emulogic Inc,** 3 Technology Way, Norwood, MA 02062. **Write 148**

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Put sight in your present system by mating your computer with our Video Graphics boards. They digitize and display information in real time from standard video cameras for MULTIBUS™ and Q-BUS™ systems... without host computer intervention.

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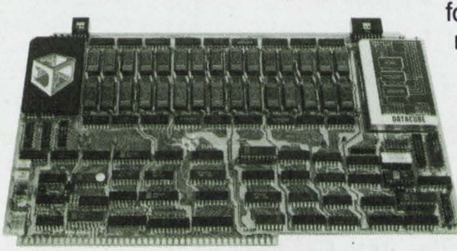
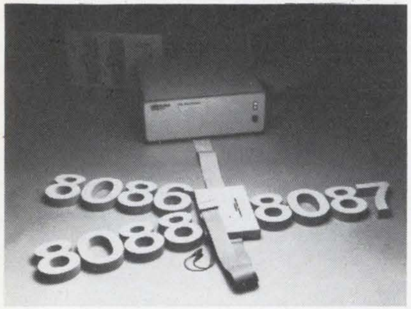


DEVELOPMENT SUPPORT

New Concept For In-Circuit Emulation

The Power Probe permits simultaneous co-processor emulation for the Intel 8086/8087 and 8088/8087 processor pairs. This makes the FutureData development system the first to provide complete software debugging and software/hardware integration capability for Intel processor pairs. The Power Probe is also capable of emulating the 8086 and 8088 separately. A Pascal compiler supporting these combinations is available. Also available is in-circuit emulation capability for the 8085 at 5MHz, the 8088 at 5MHz and the 8086 at 8MHz as independent personality modules. The Power Probe is $7400; Pascal compiler is $3200. **FutureData,** Div of GenRad Inc, 5730 Buckingham Pkwy, Culver City, CA 90230. **Write 149**



TAPE SYSTEM

Tri-Density System For PDP-11/70

This tri-density tape (800/1600/6250 bpi) subsystem supports TWE 16 emulation by replacing the RH 70 plugging directly into the 11/70 cache bus. The IPS 7016 supports reading and writing data at 125 ips and 500 ips re-wind speed. With extensive hardware error recovery, this sytem offers two track data correction and three orders of magnitude greater error recovery capability. $37,000. Also available is a 160MB Winchester disk subsystem compatible with Unibus and Q-bus. The IPS BIG BYTE supports RP/RK emulations. Unit qty price is $8350 including cables and terminators. **Information Products Systems Inc,** 6567 Rookin, Houston, TX 77074. **Write 150**

WINCHESTER FOR MDOS

10MB For Motorola Exorcisor Systems

The Winchester drive has been interfaced so that no modifications to MDOS are required and all existing MDOS based software stays alive.

The firmware which resides in the existing Exorcisor disk controller board, fools MDOS into thinking that it has 16 virtual, double sided, single density, 8″ floppy disk drives on line at any given time. All user software operates without modification as well as all MDOS software for the Exorcisor. Available for 6800 and 6809 systems and single or double sided diskette drives. $6875. **Computer System Associates Inc,** 7562 Trade St., San Diego, CA 92121. **Write 157**

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DEC

DEC 1200 BAUD PRINTERS

LA120-AA. EIA, KSR, Keyboard Only **$1,995**
LA120-BA. EIA, Keyboard & Keypad, KSR **2,075**
LA120-RA. Receive Only **1,795**

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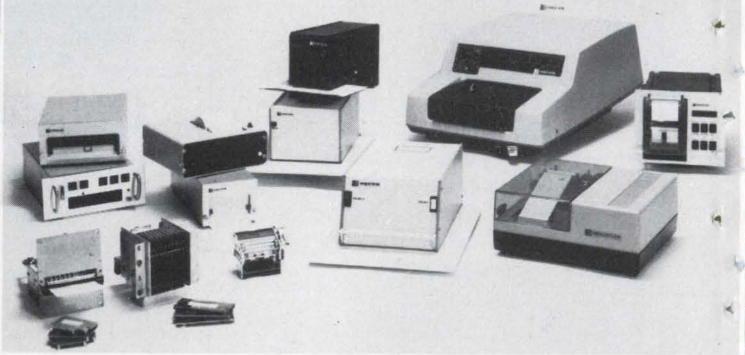
The Little Printer That Didn't.



A technician anxiously approaches the test rack early on a Monday morning. Sipping his first cup of coffee, he looks expectantly at the tape for the results of the test run over the weekend. Blank. Eyes widening, he presses the "print" button. Silence. Frantically, he searches for a reason. Then he spots it. The printer . . . is not a Hecon.

Hecon has built quality printers that you can depend on for over a decade. We can supply Impact Dot Matrix, Thermal, Electrosensitive, and Modular Impact units. From one column to eighty columns. You can specify complete printers or OEM mechanisms. We also design and build custom units.

So the choice is yours—a printer that won't or a Hecon that will.

It's got to be good. It's a Hecon. 8 9 0 HECON®

Hecon Corporation, 31 Park Road, Tinton Falls, NJ 07724
• (201) 542-9200

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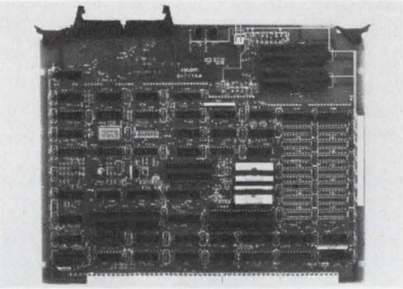
COMM CONTROLLER

4 Async Or Bit Sync Channels

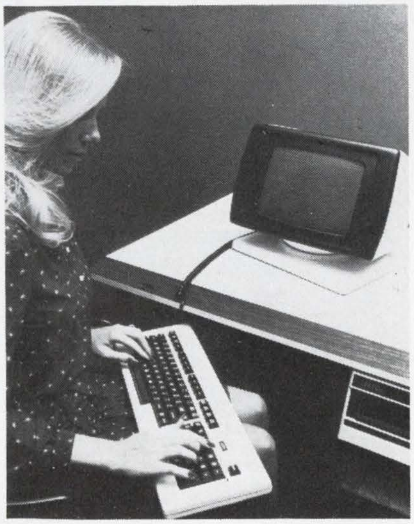
This general purpose serial communications controller allows host to host, host to 4 targets, or host to 4 terminals communications. The 1847+ is an industrial grade µP based module built to withstand electrical noise, airborne contaminants, vibration and other environmental problems. Each channel may be independently configured in bit sync record mode (SDLC), async record mode or async character mode. All 4 channels have on board variable size buffering, on board or external baud rate generation, and all 4 may be operated simultaneously. **Xycom Inc,** 750 N. Maple Rd, Saline, MI 48176. **Write 153**

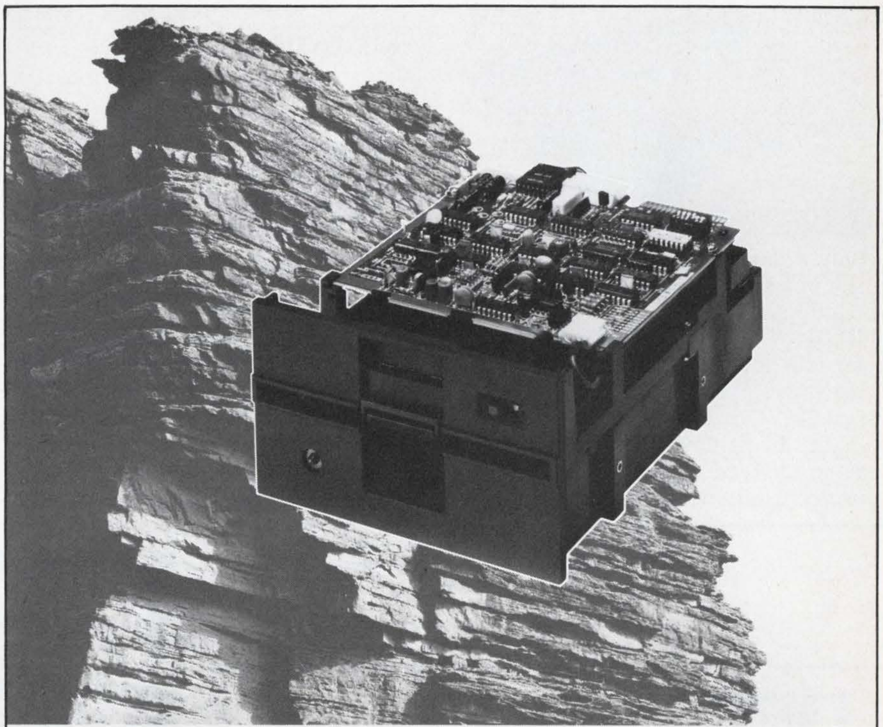


DISPLAY TERMINAL

Detached Keyboard, Green Tiltable Screen

The Altos 1 features a low-profile detached typewriter-style keyboard with 105 keys. It is connected via a 6′ cable to the rotating, tilting display, which reduces operator eyestrain through a green-phosphor screen. Thus, the keyboard/display can be configured to meet the needs of any operator and any workstation. Keyboard format capabilities are 24 lines with 80 characters per row, with two additional lines for messages and function key identification. Eight program function keys plus a special function key provide up to 96 codes. Functional command, editing and cursor keys allow full editing options as well as send and print. The display is capable of graphics line drawing and horizontal/vertical split screen with independent scrolling. It features 15 transmission baud rates from 50 to 9600 baud via a standard RS232C interface. The printer port allows data transfers at rates between 50 and 9600 baud. $995; qty discounts avail. **Altos Computer Systems,** 2360 Bering Dr, San Jose, CA 95131. **Write 154**





ROCK-SOLID FLOPPY DISK DRIVES FROM TEAC

Unique DC Spindle Drives feature our continuously-running brushless DC motor whose typical life expectancy is over 10,000 hours. Rock-stable, no electrical noise will interfere with the integrity of your data.

Superior Chassis features fiberglass reinforced polyester (FRP) which, unlike aluminum, won't stretch with heat. Extra-rugged and precision molded, the unit also has a shield to insulate the head from outside interference.

25 Years of Leadership in all magnetic recording technologies is your assurance of a quality product you can rely on. For complete information on all TEAC Rock-Solid Floppy Disk Drives (FD-50 Series) — including our one-year warranty and full technical support and service — just write:

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TEAC Corporation of America
Industrial Products Division
7733 Telegraph Road, Montebello, CA 90640
(213) 726-8417

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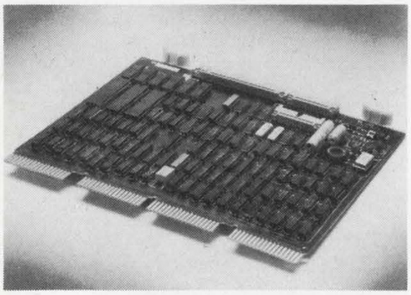
DISK CONTROLLER

Interfaces CDC Lark Drives To LSI-11s

This controller interfaces one or two CDC Lark 8MB fixed and 8MB removable media drives with LSI-11 computers. The DQ204, a self-contained quad size controller, requires only a flat ribbon cable and a single slot in any LSI based quad backplane. It offers a switch selectable choice of RL01 or RL02 software emulations, for four logical units, and is compatible with RT-11 and RSX-11 operating systems. Other features include automatic media-flaw compensation and retry on read errors, software write protect, automatic power down protection, on-board bootstrap loader for RL01/RL02 and TM-11 support with jumper selectable bootstrap address, automatic self-test, full sector data buffer for elimination of data-late errors due to DMA latency, memory addressing to 128K words, and low power consumption. $1622 in qty. **DILOG (Distributed Logic Corp),** 12800 Garden Grove Blvd, Garden Grove, CA 92643. **Write 129**



64K DYNAMIC RAM

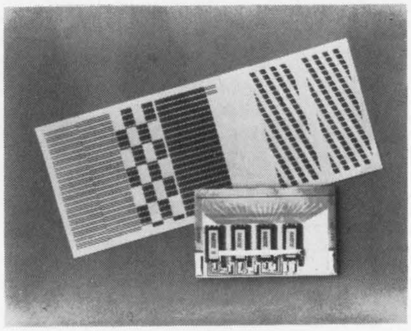
200ns RAM In Plastic Package

The 16-pin DIP is based on a specially developed compound used to protect against stringent environmental conditions and soft errors. It is targeted for high-density memory applications in PC boards assembled with automatic insertion equipment or other robotized methods that reduce production and testing costs. The MSM 3764-20RS is being offered in a special "Byte Kit" of eight 64K DRAMs with a data sheet and a summary of testing results for $64. **Oki Semiconductor Inc,** 1333 Lawrence Expwy, Santa Clara, CA 95051. **Write 134**

20-COL PRINTHEAD

13 msec Line Print Speed

The KH128 is designed for instrumentation and data logging requirements. It utilizes thick film technology combined with I^2L shift registers and drive circuits mounted directly on the substrate in integrated form. 100 print elements with dimensions of 0.010 x 0.0138 inches each are arranged in 20 five element character groups. Total print width is 1.86". The printing surface is located 0.14" from the edge of the module. $85 (1000 qty). **ROHM Corp,** PO Box 19515, Irvine, CA 92713. **Write 136**



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DEC CRT'S

VT101-AA. EIA, Non Upgradeable . . . . $ 995
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And Offers Outstanding Reliability for Minicomputer Users.

The MaxiRam Memory Storage System significantly increases throughput while virtually eliminating maintenance, repairs and downtime. With no latency time, this **high-speed, solid-state disc replacement,** in core or semiconductor, can cut lengthy 'wait' times and substantially increase user productivity. Ideal for swapping, scratch files, overlay storage, process control, etc. Let us show you how the MaxiRam System can improve your performance. With high reliability!

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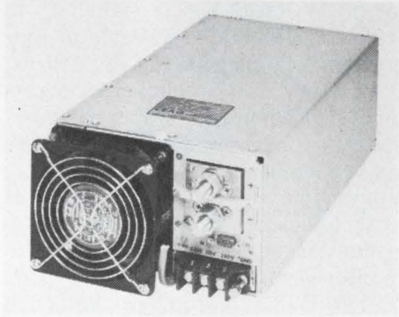
1500W SWITCHERS

Mil Style Modular Packaging

These modular, single-output switching power supplies provide outputs from 2 to 48V DC with high current ratings. Up to 1500 W of output power is available from Model SP4001 commercial units. Military-style packaging contributes to high reliability and long life. Combined line and load regulation is 0.25% and efficiency is at least 70% for all models. Input is single-phase, 115V or 230V, 57 to 63 Hz line power. All models can operate at full load over the entire 0 to 71° temperature range without derating. Noise, ripple and spikes are less than 100 mV, peak-to-peak. Features include minimum 30 ms holdup following power line outage and the ability to be operated in parallel. Both DC output and AC input overvoltage protection are provided along with soft-start, remote sensing and bit output. $1795 in 100+ qty. **CEAG Electric Corp,** 1324 Motor Pkwy, Hauppauge, NY 11788. **Write 142**



CATV AMPLIFIERS

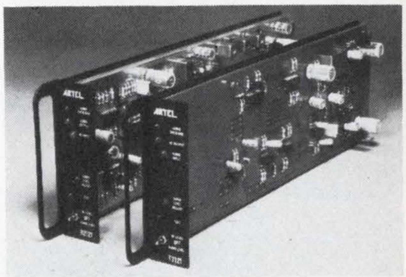
Improved Dynamic Range

CATV hybrid return amplifiers in the 5 to 200 MHz frequency range offer high dynamic range to eliminate critical fine tuning problems. The CA 4400 Series are designed for mid-split and high-split systems. They achieve a substantial improvement in dynamic range (typically 5 dB), compared with earlier models, due to the incorporation of a new-generation transistor. Three versions are available. The CA 4412 has 13 dB of gain. The CA 4418 and the CA 4422 have 18.5 dB and 22 dB of gain respectively. **TRW Semiconductors,** 14520 Aviation Blvd, Lawndale, CA 90260. **Write 145**

FIBER OPTIC SYSTEM

Dual Channel Audio Capability

The SL-2000 is capable of simultaneously transmitting broadcast quality video and two channels of broadcast quality audio over a single optical fiber. The T-2121/R-2121 audio subcarrier module set plugs directly into the SL-2000 multichannel video/audio card frame to deliver a second independent 20 KHz broadcast quality audio channel for applications including studio-transmitter links, satellite up/down links and secure video/audio local networks such as teleconferencing. **Artel Communications Corp,** PO Box 100, W. Side Station, Worcester, MA 01602. **Write 141**



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1 For FASTER service attach old mailing label in space below.

If mailing label is not available, print your old company name and address in this box.

Please allow six weeks for change to take effect

2 Print NEW business address here

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STATE ZIP

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A Smaller Alternative.

Need a quick, easy way to talk to a computer? Here's a hand-held, fully portable computer terminal that gives instant access to any ASCII transmitting data system with an RS232 interface. It's the revolutionary G.R. Electronics Pocket Terminal.

The silent, solid-state terminal has a 40-key, positive click-response keyboard. From its 32-character internal memory it displays eight bright 16-segment LED characters through a one-line window.

You may select from two alternate display modes. Entries may be in any format required, and all memory data can be edited as desired.

Miniature switches allow selection of these options • Single or dual stop bits • Parity bit SET/RESET/EVEN/ODD • 300/110 baud transmission rates • Control code response ENABLE/DISABLE.

- Compact, Lightweight, Fully Portable
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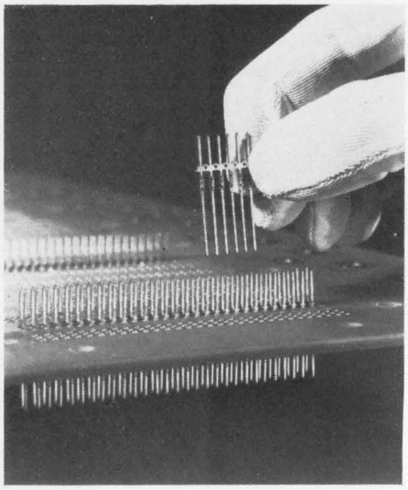
FEED-THRU CONTACT

Eliminates Damaging Multilayer PC Board

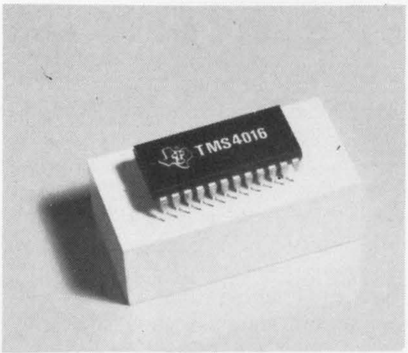
The Delta-C section compliant press-fit feed-thru contact eliminates the possibility of damaging the plated-thru hole of multilayer PC boards. The contact can be inserted into a printed circuit, requiring a finished hole size of ±.003" rather than the conventional hole size of ±.002". Users include computer, telecommunications, aerospace and industrial system equipment manufacturers. Contact spacing available are .100, .125, .150, .156 and .200 centers. The Alloy 510 contacts are available with Gold, Gold Selective, Alloy 725 unplated, Selective Gold plated or Solder Plate. From 3-½ to 7 cents per contact depending upon plating. **Methode Electronics Inc,** Connector Div, 7447 W. Wilson Ave, Chicago, IL 60656. **Write 144**



UPGRADED 16K STATIC RAM

Maximum Access/Minimum Cycle Times of 120ns

An upgraded version of the TMS4016 16K static RAM, the TMS4016NL, has improved design features that allow it to offer maximum access/minimum cycle times as fast as 120 ns, compared to 150 ns for the previous version. It also has a maximum power dissipation of only 385 mW compared to 495 mW for the previous part. Organized as 2K x 8, the TMS4016NL features fully static operation and EPROM/ROM compatibility. The latter feature gives designers complete flexibility in partitioning system memory, including the ability to prototype in RAM before switching to ROM or EPROM. Available in four performance ranges: 120 ns, 150 ns, 200 ns, and 250 ns maximum access times and minimum R/W cycle times. Packaged in a standard 24-pin, 600-mil-wide plastic package. Operating temperature is 0 to 70°C. From $9.25 to $15.90 ea. in 100 qty. **Texas Instruments Inc,** Central Literature Response Center (SC-356), PO Box 202129, Dallas, TX 75220. **Write 140**



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DEC DEC 300 BAUD PRINTERS

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LA34-RA	EIA, Receive Only	850
LA38-GA	EIA, KP & Tractor	1,000
LA38-HA	EIA, KP, Tractor & Stand	1,100
LA38-AA	EIA, KP, Forms & Tractor	1,150

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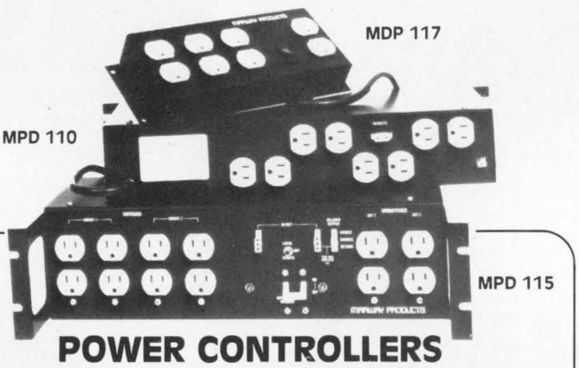

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- Interchangeable with DEC MODEL 861
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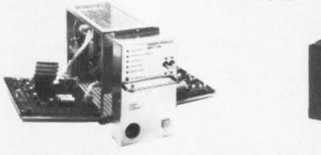
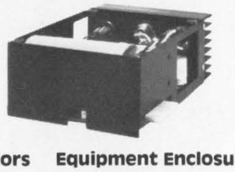
- DEC 869 Compatible
- MPD 208 90 Amps
- MPD 416 45 Amps (Not Shown Above)

ALSO





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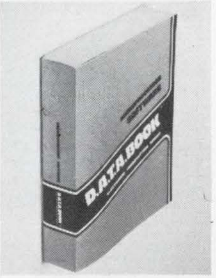
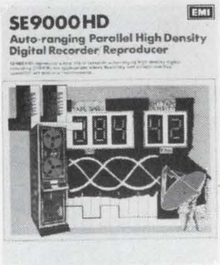


Microprocessor Software And Vendors. Published twice a year, the software data is organized by general type of software package with the package identified by the µP upon which it will operate, then by the manufacturer's titles. Includes resident, cross system, systems support and application programs. Pre-publication discount of 20% off the July 1982 price of $120.

D.A.T.A., Inc. Write 256

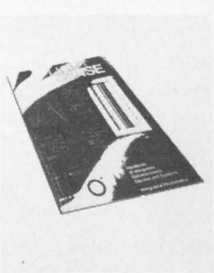

SE9000HD
EMI
Auto-ranging Parallel High Density Digital Recorder Reproducer

Auto-Ranging Parallel Digital Recorder. Described is the SE9000HD auto-ranging parallel high density digital recorder/reproducer. The heart of the system is a new recording format which extends both ends of the data-rate spectrum. A 3 position-modulation (3PM) coding scheme permits data to be packed at densities up to 45 Kbpi. The low frequency limit is reduced to less than 10 Kbps (per track). 10 pp.

EMI Technology Write 257

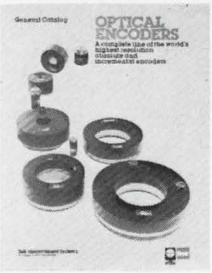
Data Communications/Telecommunications. Halcyon's entire selection of data communications and telecommunications equipment is illustrated in this 6 pp. Product Catalog Summary. With full-color photographs of each instrument, the catalog provides an overview of their three product lines.

Halcyon Communications Write 259



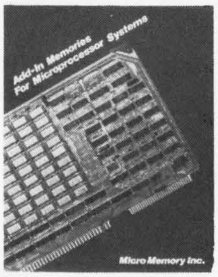
Optoelectronics Designers Handbook. Describes over 50 applications for detectors ranging from single element diodes to the more advanced 2048 arrays. The first 10 chapters cover a basic review of optics and light measurement; manufacturing technology; and essential operating photodiode characteristics such as sensitivity and noise. Included are graphs, charts, tables, and descriptive circuit and logic diagrams. 150 pp, $12.95.

Integrated Photomatrix Write 260


General Catalog
OPTICAL ENCODERS
A complete line of the world's highest resolution absolute and incremental encoders

Absolute And Incremental Encoders. This 6 pp. Optical Encoder Catalog lists the RA Series of Absolute and the RI Series of Incremental Rotary Optical Shaft Angle Encoders. A handy Resolution Equivalents chart offers Binary and Decimal data, and all encoders shown are available with many options for special applications.

Itek MSD Write 261



Add-In Memories. Included are memories for Multibus, EXORciser and LSI-11 µP systems. Key features of the memory boards are listed under each type. Parameters include cycle time, access time, storage capacity, power monitoring, and write protect control. Catalog, 6 pp.

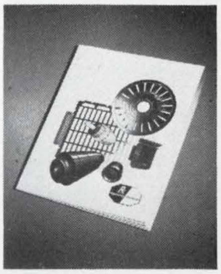
Micro Memory Write 263

Linear Voltage Regulators. This 16 pp. application note provides detailed design information on a wide variety of voltage reference circuits and regulators. In total, 18 circuits are discussed with schematics, brief descriptions, and performance data. Circuits include bandgap voltage references, Zener diode references, series and shunt regulators, and positive and negative regulators.

Interdesign Write 262

Molding Compounds. The physical, molding and performance characteristics of diallyl phthalate (DAP) and phenolic molding compounds are described. These thermoset plastics are used in automotive, electronic and electrical applications. The brochure examines the mechanical properties of the compounds, lists typical physical properties in chart form and shows the results of creep testing on several thermoset and thermoplastic materials. 8 pp.

Rogers Write 264

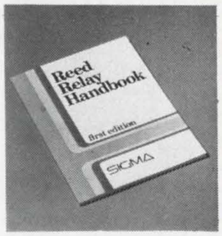


Telecommunications Networks and Equipment. Covering current trends in hardcopy message transmission, the brochure contains brief overviews on the revolution in message communications and its causes, how communication networks evolve, advantages and problems inherent in different types of networks and the evolution of electronic mail. It also details considerations in selecting telecommunications equipment. 12 pp.

Sidereal Write 265

Reed Relay Handbook. Contains technical information including: how a reed relay works, applying dry reed relays, applying mercury-wetted reed relays, testing procedures, definitions of relay terms, and physical and electrical characteristics for all standard Sigma reed relay products. Handbook ES152.

Sigma Instruments Write 266



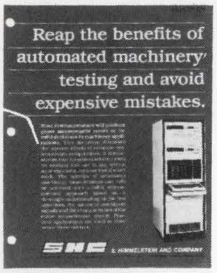
Semipack Thyristor/Diode Modules. Semipack power modules, for use in controlling electric motors (from 1 to 200 hp) and other power applications are covered. Includes a wide variety of electrical, mechanical and thermal specifications and data. Circuit diagrams, dimension drawings, definitions, fuse recommendations, snubber networks, application notes and 38-pages of ratings curves are also included. Catalog, 66 pp.

Semikron International Write 267

Matrix Boards. This product brochure provides detailed information on matrix boards and their applications. Featured are three different size boards: .250, 4mm and .100″ centers. Also shown are single, two layer and multi-deck construction. Matrix boards programming is applicable to µP projects as well as test equipment, machine controls, and signal monitoring.

Sealectro Write 268

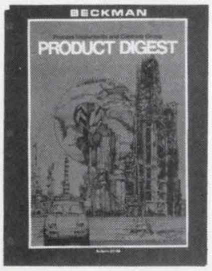
New Literature


Reap the benefits of automated machinery testing and avoid expensive mistakes.
S. HIMMELSTEIN AND COMPANY

Automated Machinery Testing. This 24 pp. booklet discusses the adverse effects of common system design compromises. Emphasis is placed on achieving a valid approach based on a thorough understanding of the test objectives,the nature of machinery signals and the measurement system characteristics.
S. Himmelstein **Write 269**

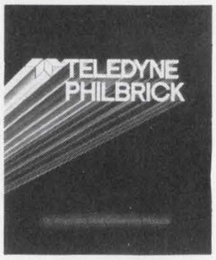
Model 6000A Memory Tester
Model 6000A Memory Tester
Model 6000A Memory Tester
TestMaster

6000A Memory Tester. The 6 pp. brochure refers to the tester in general terms, then lists features and specifications in detail. Applications and options are listed along with information on user training and the company warranty. Architecture is illustrated in a block diagram while a line drawing and photographs show how the elements combine to produce a memory tester.
TestMaster **Write 271**



Process Products. The product digest describes process analytical and control instrumentation, air and water quality products, exhaust analysis instruments and systems, and automotive test instruments. It highlights product features and references available literature describing in detail each product model. Bulletin 4210A, 16 pp.
Beckman Instruments **Write 273**

OP AMPS And Data Converters. This 272 pp. manual presents applications hints, selection guides and full specs for Teledyne Philbrick's line of modular and microcircuit signal conditioning products. It details the performance and usage of a large selection of devices including wideband and power operational amplifiers; A/D and D/A converters; logarithmic, instrumentation and sample/hold amplifiers.
Teledyne Philbrick **Write 272**



Switching Power Supplies. This 4 pp. brochure lists 26 different units. They include single, dual and triple output voltages from 5,12,15 and up to 24 volts DC. Power output ranges are from 15 W up to 100 W. The entire line is designed especially for mini/micro-computer applications.
Calex Mfg. **Write 286**

AC Line Regulators. An introductory page discusses power line problems and various solutions. Through use of sync solid state switching technology, Deltron Line Regulators control under and over voltages and brownouts and protect critical electronic equipment from power fluctuations. Bulletin 141, 6 pp.
Deltron **Write 276**

NEW FROM DELTRON
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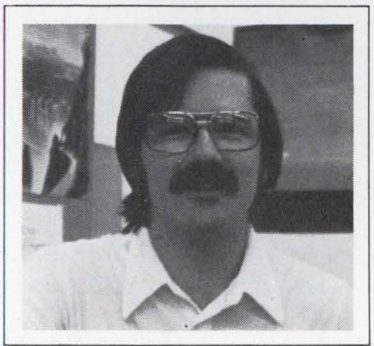
Is Error Detection/Correction Needed In 64K RAM Board Designs?

This month, the opinion page is handed over to several representatives of leading semiconductor and board level manufacturers to express their thoughts on the role of EDC in memory board design. Here's what they said:

Future Memory Designs Will All Incorporate EDAC

by Warren K. Miller
Advanced Micro Devices, Sunnyvale, CA



The engineering decision to use Error Detection and Correction (EDAC) circuitry, like all engineering decisions, should be made on the basis of a cost versus benefit analysis.

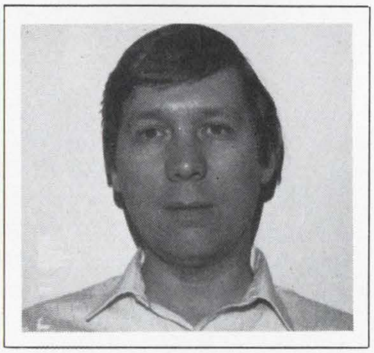
The cost analysis is quite straightforward. EDAC circuitry will add 19% to the memory chip cost in a 32-bit system and a couple of hundred dollars in overhead circuitry (two Am2960's and eight Am2961's, again for a 32-bit system). The other main cost associated with EDAC is reflected in the increase in memory access time, about 60ns for a 32-bit error detect.

The benefits of EDAC circuitry vary dramatically from application to application. In some cases, EDAC allows a manufacturer to specify a mean time between failure (MTBF) superior to the competition. This alone may be worth the cost in some cases. A more dramatic case would be in an air traffic control system or a nuclear power plant. The cost of the memory error in these systems is incalculable. The increased reliability offered by EDAC circuitry is well worth the slight increase in memory cost.

As VLSI EDAC chips like the Am2960 reach production maturity, the cost of adding EDAC to a memory system will decline even more. At that point, the benefits of increased reliability will swamp the slight cost of EDAC. Thus, virtually every memory design will incorporate EDAC in the near future.

ECC Shouldn't Be Automatic For 64K RAM Systems

by Joe Altnether
Intel Corp., Aloha, OR



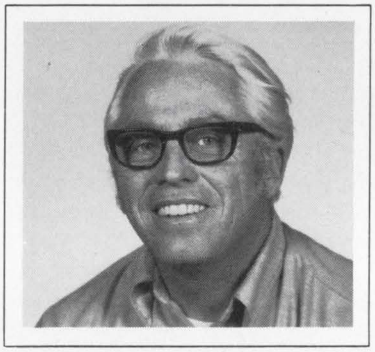
ECC should not be automatically designed into a system simply because it contains 64K RAMs. Because the incorporation of ECC costs approximately 40% more in dollars and 25% in system performance, the designer must evaluate the cost of an error against the cost of adding ECC. Error costs are usually high enough to justify ECC in systems that would jeopardize life, finances or system repairability. Whereas, ECC in a video game CRT refresh, for example, offers no advantage.

Not all applications are as well defined as the previous examples and ECC usage is not a simple decision. System reliability (MTBF) goals must be established and used as the deciding factor. Typically, a one year MTBF is sufficient for most applications. As MTBF is inversely proportional to the number of RAMs used and the RAM failure rate, memory intensive systems should incorporate ECC only to satisfy MTBF goals. Conversely, smaller memory systems cannot bear the cost and performance burden of ECC and the challenge for the designer is to obtain his MTBF goals without ECC circuitry. Recognizing that soft errors are the dominant failure mechanism, the designer must select a 64K RAM with a low soft error rate (SER) to preclude the use of ECC.

The criteria for selection is the method used by the manufacturer to achieve a low SER. The best method is to design soft error immunity inherently into the RAM. Intel chose precisely this technique, that is, to build a 64K RAM without a die coat but with cell capacitance 1.7 times larger than previous 64K RAMs. Consequently the SER is reduced to less than .1%/1KHr, therefore significantly increasing the system MTBF. As a result, many small system designs using this 64K RAM do not require ECC.

ECC Relies On Application, Not Memory Size

by Dick Brunner
Motorola Semiconductor, Austin, TX



There are some who like to use a rule of thumb number, such as any memory over ¼ Mbyte should require error correction. However, the decision to employ error detection and correction with 64K RAM board designs should primarily depend on the application and not necessarily the size of the memory.

As an example, let's look at the memory requirements for high resolution video graphics. For this application an occasional data bit error would not impact the operation of the system or the overall integrity of the screen display.

On the other hand, applications such as numerical control for milling machines, telecommunications, and data base storage for banks would require very reliable memory. Even in some of these applications, the reliability of 64K RAM components are improving such that it may not be essential to have error correction.

Of course, the question of reliability of a RAM component has become more complex with the susceptibility of high density RAMs to alpha induced soft failure. However, in the past couple of years much has been done to reduce the susceptibility of these components to alpha's. In fact, the reliability of 64K RAMs are as good if not better than presently manufactured 16K RAM parts. With comparable reliability of 16K RAMs, an upgraded redesign with 64K RAMs for the same size memory should result in a memory system four times more reliable, for the memory components only.

With this kind of reliability improvement it may be possible to upgrade a 16K memory board design with error correction to a 64K design without error correction.

Remember error correction not only requires additional memory and logic, but will also result in reduction of data throughput because of the longer cycles. Since error correction is costly not only in dollars but also performance, it should be used in applications where reliability is essential.

RAM Error Rate Dictates EDAC Use

by Peter Barratt
NEC Electronics, Natick, MA

The use of EDAC (error detection and correction) circuitry is dictated by the required error rate of the RAM board. Since the NEC μPD4164C exhibits projected soft error rate of less than 80 FITS (.008%/1K device hours), and the hard error rate is equal to or better than that for 16K's, there should be a four fold improvement in the error rate for a system using 64K's over a similar capacity design based on 16K's. By virtue of the reduction in RAM chip count, of course, if one uses a 64K RAM with a significantly worse soft error rate than the corresponding 16K, EDAC may well be called for to provide acceptable system performance. Also, this analysis does not take errors due to backplane noise, etc, into account.

If you didn't use EDAC on your 16K designs, and your system requirements haven't changed, don't bother for your 64K system and use a chip with a low soft error rate.

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```
32BIT T=XXXX C=S+0202        MEM-
C=0202               MNEMONIC [Z80]
ADRS DATA            RST    38H
                     LD     HL,2000H
FFFF FF              NOP    NZ,+3EH
004A 210020          JR     A,10H
004B 00              LD     +77H
004C 203E            DJNZ   (HL),A
004D 3E10            LD     +3DH
004E 1077            DJNZ   A
004F 77              DEC    HL
2000 103D            INC    NZ,-05H
0050 3D              JR
0051 23              EI     (HL),A
0052 20FB            LD
0053 FB              RRCA   A
004F 77              DEC    HL
2001 0F              INC
0050 3D
0051 23
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